BECKHOFF

CB3054

Manual

rev. 1.5

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Contents

0 Document History

Version	Changes
0.1	first pre-release
1.0	first complete version
1.1	- added recommendation for PCIe adapter cards - updated annex (memory map & SMB device map) - minor changes - updated GPIO connector description
1.2	improved output quality of dimensional drawings, minor changes
1.3	updated pinout COM 2-4
1.4	updated dimensional drawings
1.5	corrected LAN pinout

NOTE

1 Introduction

1.1 Notes on the Documentation

This description is only intended for the use of trained specialists in control and automation engineering who are familiar with the applicable national standards. It is essential that the following notes and explanations are followed when installing and commissioning these components.

1.1.1 Liability Conditions

The responsible staff must ensure that the application or use of the products described satisfy all the requirements for safety, including all the relevant laws, regulations, guidelines and standards.
The documentation has been prepared with care. The products described are, however, constantly under development. For that reason the documentation is not in every case checked for consistency with performance data, standards or other characteristics. None of the statements of this manual represents a guarantee (Garantie) in the meaning of § 443 BGB of the German Civil Code or a statement about the contractually expected fitness for a particular purpose in the meaning of § 434 par. 1 sentence 1 BGB. In the event that it contains technical or editorial errors, we retain the right to make alterations at any time and without warning. No claims for the modification of products that have already been supplied may be made on the basis of the data, diagrams and descriptions in this documentation.

1.1.2 Copyright

1.2 Safety Instructions

Please consider the following safety instructions and descriptions. Product specific safety instructions are to be found on the following pages or in the areas mounting, wiring, commissioning etc.

1.2.1 Disclaimer

All the components are supplied in particular hardware and software configurations appropriate for the application. Modifications to hardware or software configurations other than those described in the documentation are not permitted, and nullify the liability of Beckhoff Automation GmbH.

1.2.2 Description of Safety Symbols

The following safety symbols are used in this documentation. They are intended to alert the reader to the associated safety instructions.

ACUTE RISK OF INJURY!

If you do not adhere to the safety advise next to this symbol, there is immediate danger to life and health of individuals!

RISK OF INJURY!

If you do not adhere to the safety advise next to this symbol, there is danger to life and health of individuals!

HAZARD TO INDIVIDUALS, ENVIRONMENT, DEVICES, OR DATA!

If you do not adhere to the safety advise next to this symbol, there is obvious hazard to individuals, to environment, to materials, or to data.

NOTE OR POINTER

This symbol indicates information that contributes to better understanding.

1.3 Essential Safety Measures

1.3.1 Operator's Obligation to Exercise Diligence

The operator must ensure that

- the product is only used for its intended purpose
- the product is only operated in sound condition and in working order
- the instruction manual is in good condition and complete, and always available for reference at the location where the products are used
- the product is only used by suitably qualified and authorised personnel
- the personnel is instructed regularly about relevant occupational safety and environmental protection aspects
- the operating personnel is familiar with the operating manual and in particular the safety notes contained herein

1.3.2 National Regulations Depending on the Machine Type

Depending on the type of machine and plant in which the product is used, national regulations governing the controllers of such machines will apply, and must be observed by the operator. These regulations cover, amongst other things, the intervals between inspections of the controller. The operator must initiate such inspections in good time.

1.3.3 Operator Requirements

- Read the operating instructions

All users of the product must have read the operating instructions for the system they work with.

- System know-how

All users must be familiar with all accessible functions of the product.

1.4 Functional Range

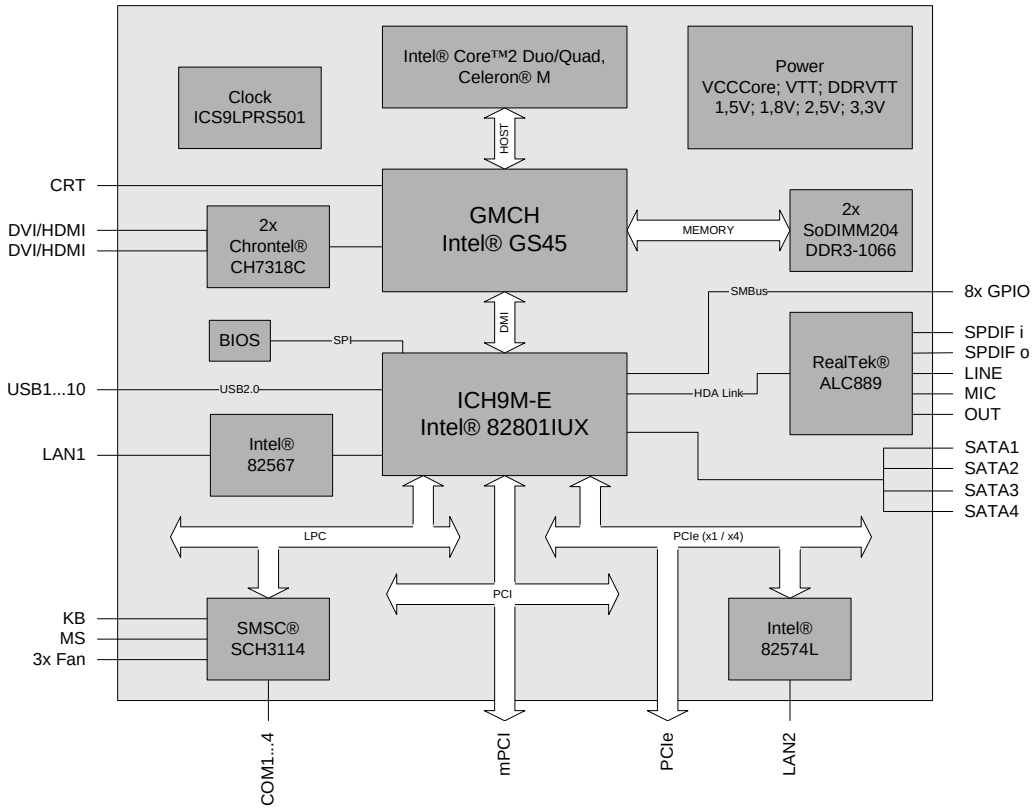
NOTE

The descriptions contained in the present documentation represent a detailed and extensive product description. As far as the described motherboard was acquired as an integral component of an Industrial PC from Beckhoff Automation GmbH, this product description shall be applied only in limited scope. Only the contractually agreed specifications of the corresponding Industrial PC from Beckhoff Automation GmbH shall be relevant. Due to several models of Industrial PCs, variations in the component placement of the motherboards are possible. Support and service benefits for the built-in motherboard will be rendered by Beckhoff Automation GmbH exclusively as specified in the product description (inclusive operation system) of the particular Industrial PC.

2 Overview

2.1 Features

The CB3054 is a highly complex 3,5-inch board which incorporates complete motherboard functionality. It's based on Intel®'s GS45 chipset combined with the ICH9M-E chip (SFF). Several CPUs are available for this board, all from Intel®'s Core™2 Duo/Core™2 Quad and Celeron® M series. Modern DDR3 technology provides top-notch memory performance, accomodating up to 8 GByte of RAM (DDR3-1066) via SO-DIMM204. It also provides a PCI bus (via mPCI connector), a PCI-Express bus (via a 2x40 pin custom connector) and additional peripheral devices such as four serial interfaces, two Gigabit Ethernet interfaces (LAN), four SATA channels, an audio interface (HDA 5.1), ten USB channels, and two DVI/HDMI connectors.



- Processor Intel® Core™2 Duo/Quad or Celeron® M
- Chipset Intel® GS45 with integrated graphics and ICH9M-E (SFF)
- Two SO-DIMM204 sockets for up to 8 GByte DDR3-1066 RAM
- PCI bus via mPCI connector
- PCI-Express bus (four x1 or one x4) via 2x40pin custom connector
- Four serial interfaces COM1 to COM4
- Two LAN interfaces Ethernet 10/100/1000 (Base-T)
- Four SATA channels
- PS2 keyboard / mouse interface
- Ten USB 2.0 interfaces
- AWARD BIOS 6.10
- CRT connection
- Two DVI/HDMI connectors
- AC97/HDA compatible sound controller with SPDIF in and out

- RTC with external CMOS battery
- 5V supply
- Format: 102 mm x 147 mm

2.2 Specifications and Documents

In making this manual and for further reading of technical documentation, the following documents, specifications and web-pages were used and are recommended.

- PCI specification
  Version 2.3 resp. 3.0
  www.pcisig.com
- Mini-PCI specification
  Version 1.0
  www.pcisig.com
- ACPI specification
  Version 3.0
  www.acpi.info
- ATA/ATAPI specification
  Version 7 Rev. 1
  www.t13.org
- USB specifications
  www.usb.org
- SM-Bus specification
  Version 2.0
  www.smbus.org
- Intel®-Chip Description
  Celeron® M, Core™ 2 Duo
  www.intel.com
- Intel® Chipset Description
  Intel® 4 Series Express Chipset Family datasheet
  www.intel.com
- Intel® Chip Description
  Intel® ICH9 Datasheet
  www.intel.com
- Intel® Chip Description
  82574L Datasheet
  www.intel.com
- Intel® Chip Description
  82567 Datasheet
  www.intel.com
- Realtek® Chip Description
  ALC885/889 Datasheet
  www.realtek.com.tw
- SMSC® Chip Description
  SCH3114 Datasheet
  www.smsc.com
  (NDA required)
- IDT® Chip Description
  ICS9LPRS501SKLF Datasheet
  www.idt.com
- Chrontel® Chip Description
  Chrontel 7318C Datasheet
  www.chrontel.com

3 Connectors

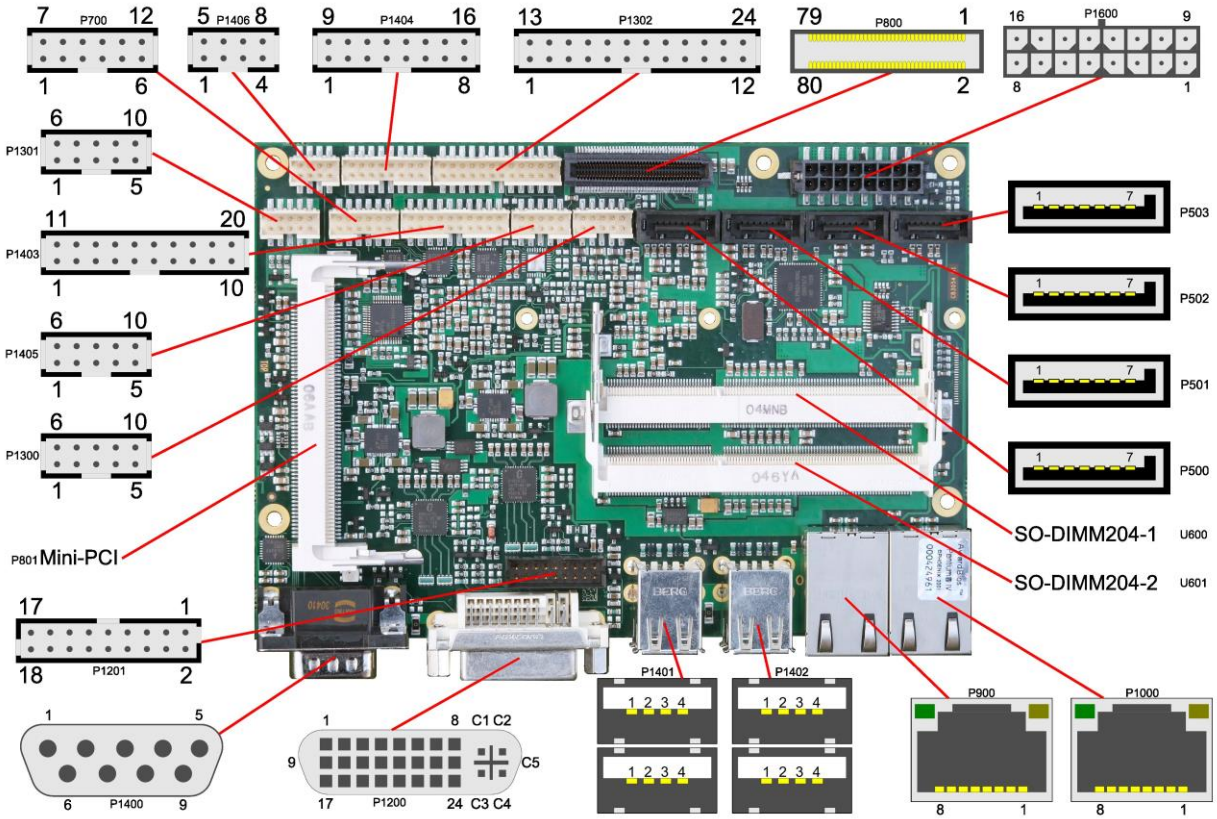
This section describes all the connectors found on the CB3054.

CAUTION

For most interfaces, the cables must meet certain requirements. For instance, USB 2.0 requires twisted and shielded cables to reliably maintain full speed data rates. Restrictions on maximum cable length are also in place for many high speed interfaces and for power supply. Please refer to the respective specifications and use suitable cables at all times.

3.1 Connector Map

Please use the connector map below for quick reference. Only connectors on the component side are shown. For more information on each connector refer to the table below.



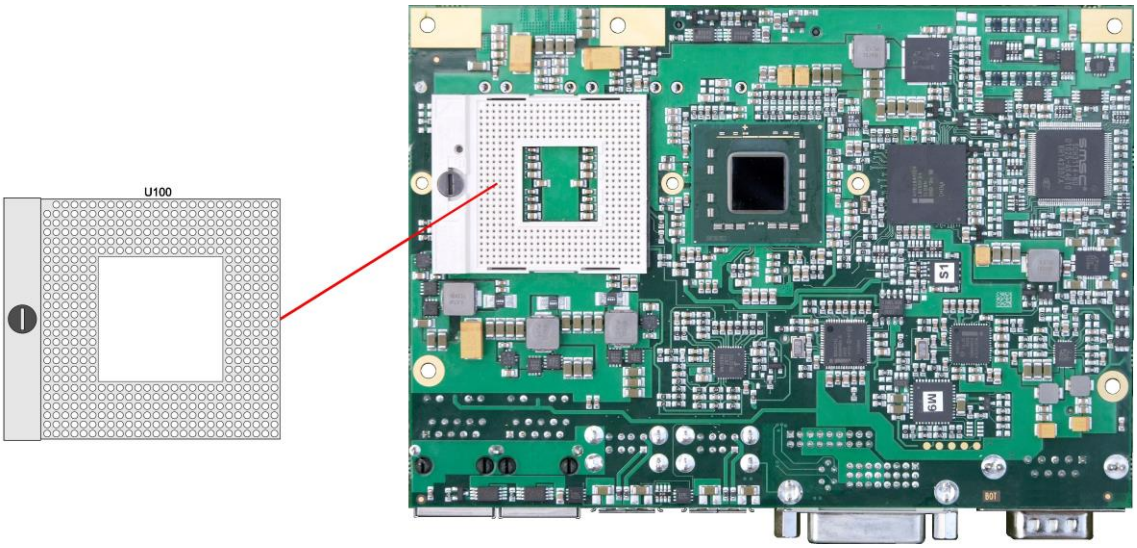
Ref-No.	Function	Page
P500/1/2/3	"SATA Interfaces"	p. 30
U600/1	"Memory"	p. 20
P700	"GPIO"	p. 38
P800	"PCI-Express"	p. 34
P801	"Mini-PCI"	p. 36
P900/1000	"LAN"	p. 28
P1200	"VGA/DVI"	p. 23
P1201	"DVI/HDMI"	p. 25
P1301	"Audio"	p. 29
P1302	"System"	p. 19
P1400	"Serial Interface COM1"	p. 31
P1403/5	"Serial Ports COM2 through COM4"	p. 32
P1401/2	"USB 1-4"	p. 26
P1404/6	"USB 5-10"	p. 27
P1300	"Fan Connectors"	p. 39
P1600	"Power Supply"	p. 18

3.2 CPU Socket

The CB3054 board has an mPGA479M CPU socket accomodating certain versions of the following types of processors manufactured by Intel®: Celeron® M, Core™2 Duo and Core™2 Quad. The mPGA479M is a ZIF (Zero Insertion Force) socket, which means that you can insert the processor without there being any resistance. There is only one orientation in which the processor will fit into the socket. Once the processor is in place the fastening screw must be tightened to ensure proper electrical contact.
The package type allows a maximum die temperature of 100 degrees Celsius and accords highest possible security even in rough environment.
The processor includes a second level cache of up to 6 MByte, depending on which model is used. Furthermore the processors offer many features known from the desktop range such as MMX2, serial number, loadable microcode etc.

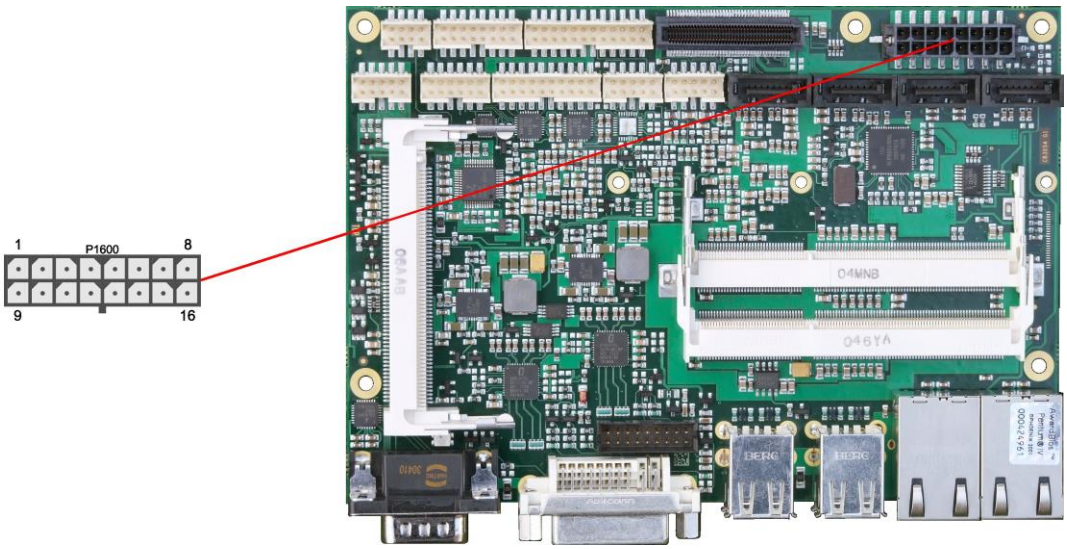
NOTE

Processors must be ordered separately. The board ships without a CPU.



3.3 Power Supply

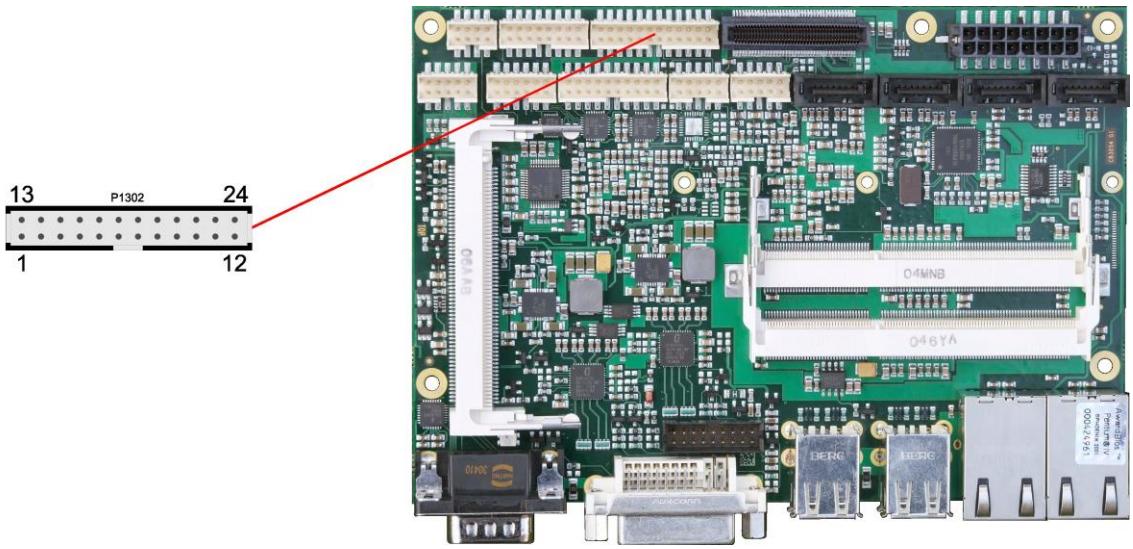
The power supply of the hardware module is realized via a 2x8-pin connector (Molex PS 43045-1619, mating connector: Molex PS 43025-16xx). The 12 volt supply is needed for PCI-Express cards and for the fan connector. COM3 RXD and TXD can also be used for connecting a second power supply unit, e. g. for UPS. As an ordering option SMBus signals SCL/SDA can be provided (replacing COM3 TXD/RXD).



Description	Name	Pin		Name	Description
COM3 transmit data	TXD	1	9	RXD	COM3 receive data
PSU on	PS-ON	2	10	PWRGD	Powergood
powerbutton PSU	PWRBTN#	3	11	SVCC	standby-supply 5V
12 volt supply	12V	4	12	12V	12 volt supply
ground	GND	5	13	GND	ground
ground	GND	6	14	GND	ground
5 volt supply	VCC	7	15	VCC	5 volt supply
5 volt supply	VCC	8	16	VCC	5 volt supply

3.4 System

A number of signals for system control and for SMBus communication are provided through a 2x12 pin connector (FCI 98424-G52-24LF, mating connector FCI 90311-024LF). This connector combines signals for power button, reset, keyboard, speaker, and several LEDs such as harddisk LED, and suspend LED, and three additional LEDs which are driven by GPIOs. Of these three GPIO-LEDs, LED1 and LED2 are already provided with a series resistor. SMBus capable devices can also be connected.

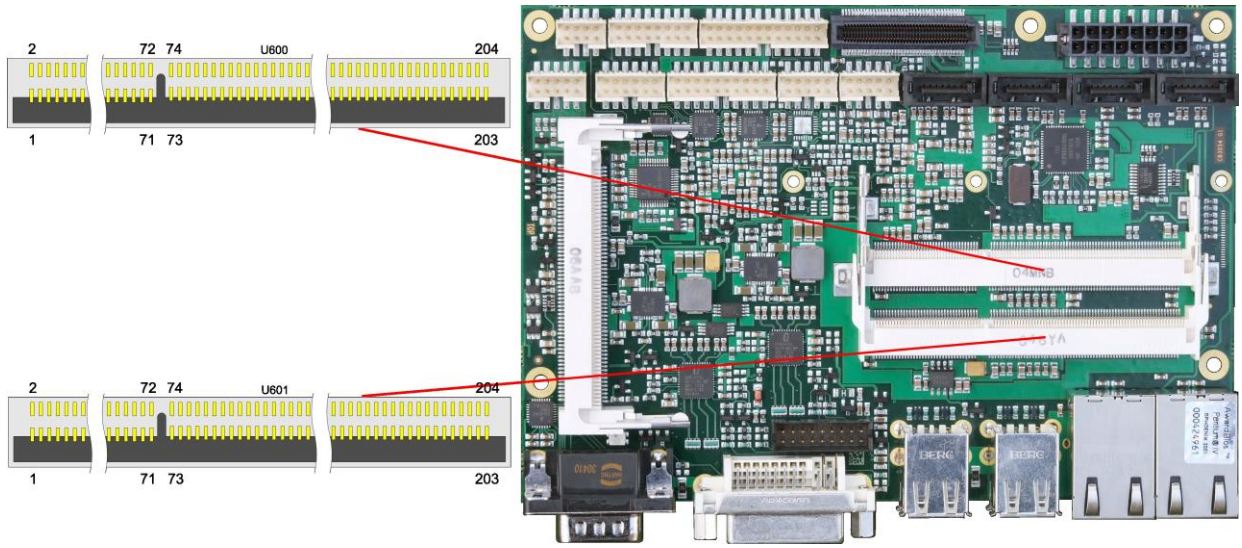


Pinout 2x12pin connector:

Description	Name	Pin		Name	Description
ground	GND	1	13	3.3V	3.3V supply
reset to ground	RSTBTN#	2	14	PWRBTN#	on/suspend button
LED suspend / ACPI	S-LED	3	15	S3.3V	standby supply 3.3V
LED harddisk	SATALED	4	16	GPIOLED3	LED GPIO device 3
LED GPIO device 1	GPIOLED1	5	17	BATT	battery
LED GPIO device 2	GPIOLED2	6	18	SMBALERT#	SMB alert
SMB Clock	SMBCLKEX	7	19	SMBDATEX	SMB data
speaker to 5V	SPEAKER	8	20	SVCC	standby supply 5V
keyboard clock	KCLK	9	21	KDAT	keyboard data
ground	GND	10	22	VCC	5V supply
ground	GND	11	23	VCC	5V supply
ground	GND	12	24	VCC	5V supply

3.5 Memory

Conventional SO-DIMM204 memory modules, as familiar from notebook computers, are used to equip the board with memory. For technical and mechanical reasons it is possible that particular memory modules cannot be employed. Please ask your distributor for recommended memory modules.
With currently available SO-DIMM204 modules a memory extension up to 8 GByte is possible (DDR3-1066).
All timing parameters for different memory modules are automatically set by BIOS.



Pinout SO-DIMM204:

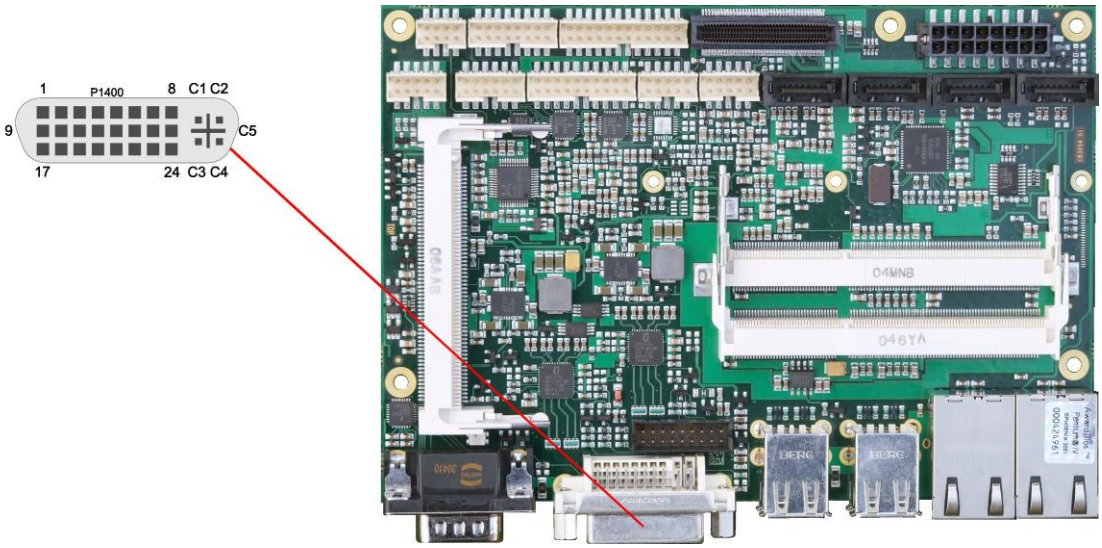
Description	Name	Pin		Name	Description
memory reference current	REF-DQ	1	2	GND	ground
ground	GND	3	4	DQ4	data 4
data 0	DQ0	5	6	DQ5	data 5
data 1	DQ1	7	8	GND	ground
ground	GND	9	10	DQS0#	data strobe 0 -
data mask 0	DM0	11	12	DQS0	data strobe 0 +
ground	GND	13	14	GND	ground
data 2	DQ2	15	16	DQ6	data 6
data 3	DQ3	17	18	DQ7	data 7
ground	GND	19	20	GND	ground
data 8	DQ8	21	22	DQ12	data 12
data 9	DQ9	23	24	DQ13	data 13
ground	GND	25	26	GND	ground
data strobe 1 -	DQS1#	27	28	DM1	data mask 1
data strobe 1 +	DQS1	29	30	RESET#	Reset
ground	GND	31	32	GND	ground
data 10	DQ10	33	34	DQ14	data 14
data 11	DQ11	35	36	DQ15	data 15
ground	GND	37	38	GND	ground
data 16	DQ16	39	40	DQ20	data 20
data 17	DQ17	41	42	DQ21	data 21
ground	GND	43	44	GND	ground
data strobe 2 -	DQS2#	45	46	DM2	data mask 2
data strobe 2 +	DQS2	47	48	GND	ground
ground	GND	49	50	DQ22	data 22

Description	Name	Pin		Name	Description
data 18	DQ18	51	52	DQ23	data 23
data 19	DQ19	53	54	GND	ground
ground	GND	55	56	DQ28	data 28
data 24	DQ24	57	58	DQ29	data 29
data 25	DQ25	59	60	GND	ground
ground	GND	61	62	DQS3#	data strobe 3 -
data mask 3	DQM3	63	64	DQS3	data strobe 3 +
ground	GND	65	66	GND	ground
data 26	DQ26	67	68	DQ30	data 30
data 27	DQ27	69	70	DQ31	data 31
ground	GND	71	72	GND	ground
clock enables 0	CKE0	73	74	CKE1	clock enables 1
1.5 volt supply	1.5V	75	76	1.5V	1.5 volt supply
reserved	N/C	77	78	(A15)	reserved
SDRAM bank 2	BA2	79	80	A14	address 14
1.5 volt supply	1.5V	81	82	1.5V	1.5 volt supply
address 12 (burst chop)	A12/BC#	83	84	A11	address 11
address 9	A9	85	86	A7	address 7
1.5 volt supply	1.5V	87	88	1.5V	1.5 volt supply
address 8	A8	89	90	A6	address 6
address 5	A5	91	92	A4	address 4
1.5 volt supply	1.5V	93	94	1.5V	1.5 volt supply
address 3	A3	95	96	A2	address 2
address 1	A1	97	98	A0	address 0
1.5 volt supply	1.5V	99	100	1.5V	1.5 volt supply
Clock 0 +	CK0	101	102	CK1	clock 1 +
Clock 0 -	CK0#	103	104	CK1#	clock 1 -
1.5 volt supply	1.5V	105	106	1.5V	1.5 volt supply
address 10 (auto precharge)	A10/AP	107	108	BA1	SDRAM bank 1
SDRAM Bank 0	BA0	109	110	RAS#	row address strobe
1.5 volt supply	1.5V	111	112	1.5V	1.5 volt supply
write enable	WE#	113	114	S0#	chip select 0
column address strobe	CAS#	115	116	ODT0	on die termination 0
1.5 volt supply	1.5V	117	118	1.5V	1.5 volt supply
address 13	A13	119	120	ODT1	on die termination 1
Chip Select 1	S1#	121	122	N/C	reserved
1.5 volt supply	1.5V	123	124	1.5V	1.5 volt supply
reserved	(TEST)	125	126	REF-CA	reference current
ground	GND	127	128	GND	ground
data 32	DQ32	129	130	DQ36	data 36
data 33	DQ33	131	132	DQ37	data 37
ground	GND	133	134	GND	ground
data strobe 4 -	DQS4#	135	136	DQM4	data mask 4
data strobe 4 +	DQS4	137	138	GND	ground
ground	GND	139	140	DQ38	data 38
data 34	DQ34	141	142	DQ39	data 39
data 35	DQ35	143	144	GND	ground
ground	GND	145	146	DQ44	data 44
data 40	DQ40	147	148	DQ45	data 45
data 41	DQ41	149	150	GND	ground
ground	GND	151	152	DQS5#	data strobe 5 -
data mask 5	DQM5	153	154	DQS5	data strobe 5 +
ground	GND	155	156	GND	ground
data 42	DQ42	157	158	DQ46	data 46
data 43	DQ43	159	160	DQ47	data 47

Description	Name	Pin		Name	Description
ground	GND	161	162	GND	ground
data 48	DQ48	163	164	DQ52	data 52
data 49	DQ49	165	166	DQ53	data 53
ground	GND	167	168	GND	ground
data strobe 6 -	DQS6#	169	170	DQM6	data mask 6
data strobe 6	DQS6	171	172	GND	ground
ground	GND	173	174	DQ54	data 54
data 50	DQ50	175	176	DQ55	data 55
data 51	DQ51	177	178	GND	ground
ground	GND	179	180	DQ60	data 60
data 56	DQ56	181	182	DQ61	data 61
data 57	DQ57	183	184	GND	ground
ground	GND	185	186	DQS7#	data strobe 7 -
data mask 7	DQM7	187	188	DQS7	data strobe 7 +
ground	GND	189	190	GND	ground
data 58	DQ58	191	192	DQ62	data 62
data 59	DQ59	193	194	DQ63	data 63
ground	GND	195	196	GND	ground
SPD address 0	SA0	197	198	EVENT#	Event
3.3 volt supply	3.3V	199	200	SDA	SMBus data
SPD address 1	SA1	201	202	SCL	SMBus clock
termination current	VTT	203	204	VTT	termination current

3.6 VGA/DVI

The module is equipped with a standard DVI-I-connector, which can be used to connect a DVI capable device, a standard VGA monitor or an HDMI capable device. External cable adapters that convert from DVI to VGA or HDMI are required to connect standard VGA or HDMI devices.



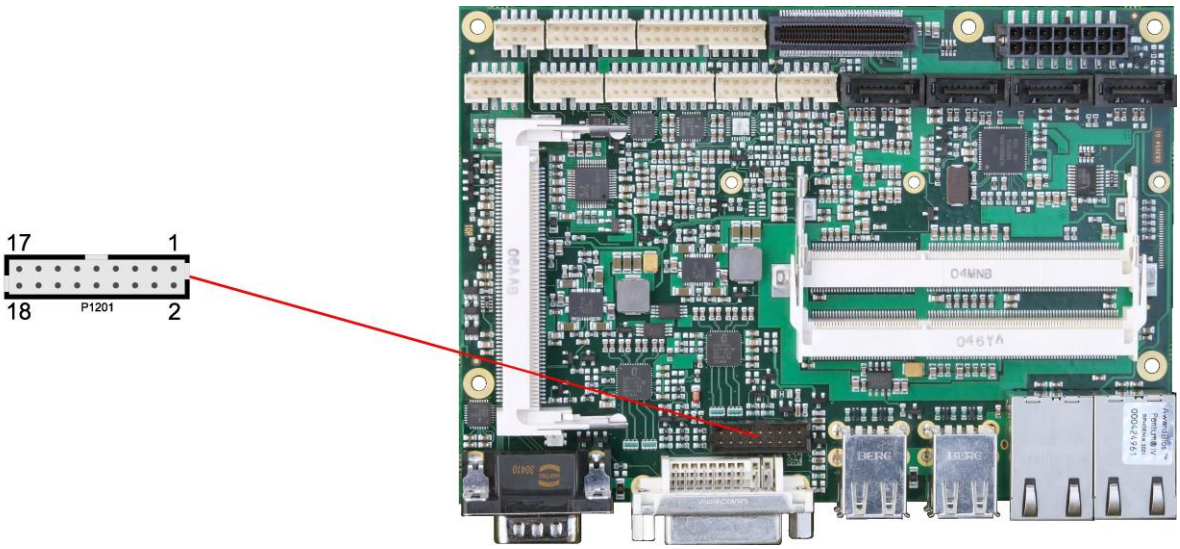
Pinout DVI-I:

Pin	Name	Description
1	TMDSDAT2#	DVI data 2 -
2	TMDSDAT2	DVI data 2 +
3	GND	ground
4	N/C	reserved
5	N/C	reserved
6	DDC CLK	DDC clock (DVI/VGA)
7	DDC DAT	DDC data (DVI/VGA)
8	VSYNC	VGA vertical sync
9	TMDSDAT1#	DVI data 1 -
10	TMDSDAT1	DVI data 1 +
11	GND	ground
12	N/C	reserved
13	N/C	reserved
14	VCC	5 volt supply
15	GND	ground
16	HP_DETECT	hot plug detect
17	TMDSDAT0#	DVI data 0 -
18	TMDSDAT0	DVI data 0 +
19	GND	ground
20	N/C	reserved
21	N/C	reserved
22	GND	ground
23	TMDS CLK	DVI clock
24	TMDS CLK#	DVI clock
C1	RED	VGA red
C2	GREEN	VGA green
C3	BLUE	VGA blue
C4	HSYNC	VGA horizontal sync

Pin	Name	Description
C5	GND	ground

3.7 DVI/HDMI

The CB3054 provides a second DVI interface which is realized as a 2x9pin header. Analog VGA is not available on this connector. However, an HDMI device can be connected.

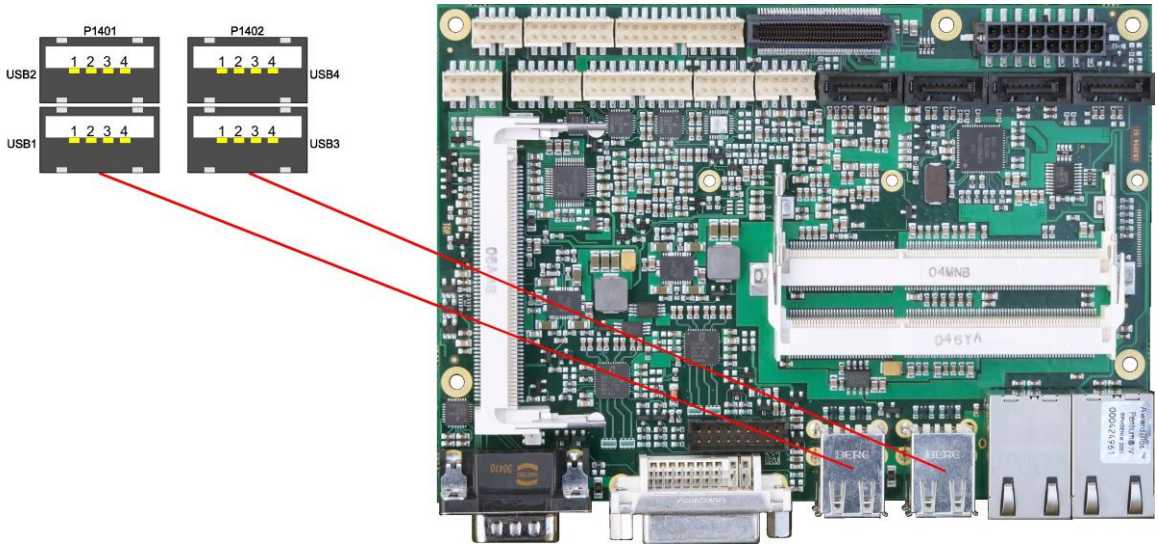


Pinout 2x9pin connector DVI/HDMI:

Description	Name	Pin		Name	Description
HDMI panel detected	HPD_SINK	1	2	N/C	reserved
SMBus clock (DDC)	SCL_SINK	3	4	SDA_SINK	SMBus dat (DDC)
5 volt supply	VCC	5	6	GND	ground
ground	GND	7	8	TMDS_CLK#	DVI clock -
DVI data 0 -	TMDS_D0#	9	10	TMDS_CLK	DVI clock +
DVI data 0 +	TMDS_D0	11	12	GND	ground
ground	GND	13	14	TMDS_D1#	DVI data 1 -
DVI data 2 -	TMDS_D2#	15	16	TMDS_D1	DVI data 1 +
DVI data 2 +	TMDS_D2	17	18	GND	ground

3.8 USB 1-4

The hardware module has ten USB channels four of which (USB1 to USB4) are available as standard USB connectors.
The USB channels support USB 2.0. You may note that the setting of USB keyboard or USB mouse support in the BIOS-setup is only necessary and advisable, if the OS offers no USB-support. BIOS-setup can be changed with a USB keyboard without enabling USB keyboard support. Running Windows with these features enabled may lead to significant performance or functionality limitations.
Every USB interface provides up to 500 mA current and is protected by an electronically resettable fuse.

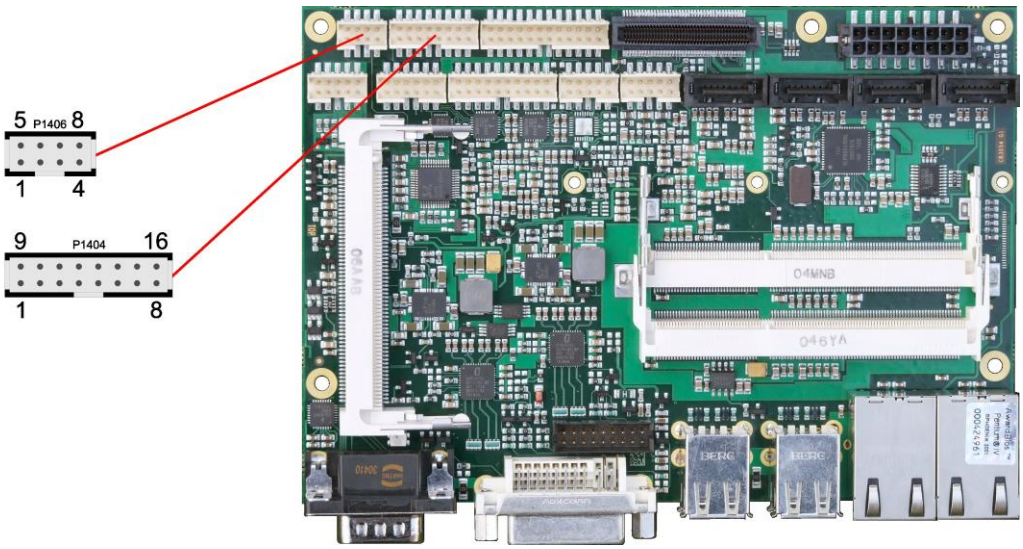


Pinout USB connector for channel X:

Pin	Name	Description
1	VCC	5 volt for USBX
2	USBX#	minus channel USBX
3	USBX	plus channel USBX
4	GND	ground

3.9 USB 5-10

The USB channels 5 to 10 are provided via two connectors, one of which is 2x4pin (FCI 98424-G52-08LF, mating connector FCI 90311-08LF), the other 2x8pin (FCI 98424-G52-16LF, mating connector FCI 90311-016LF).
The USB channels support USB 2.0. You may note that the setting of USB keyboard or USB mouse support in the BIOS-setup is only necessary and advisable, if the OS offers no USB-support. BIOS-setup can be changed with a USB keyboard without enabling USB keyboard support. Running Windows with these features enabled may lead to significant performance or functionality limitations.
Every USB interface provides up to 500 mA current and is protected by an electronically resettable fuse.



Pinout USB

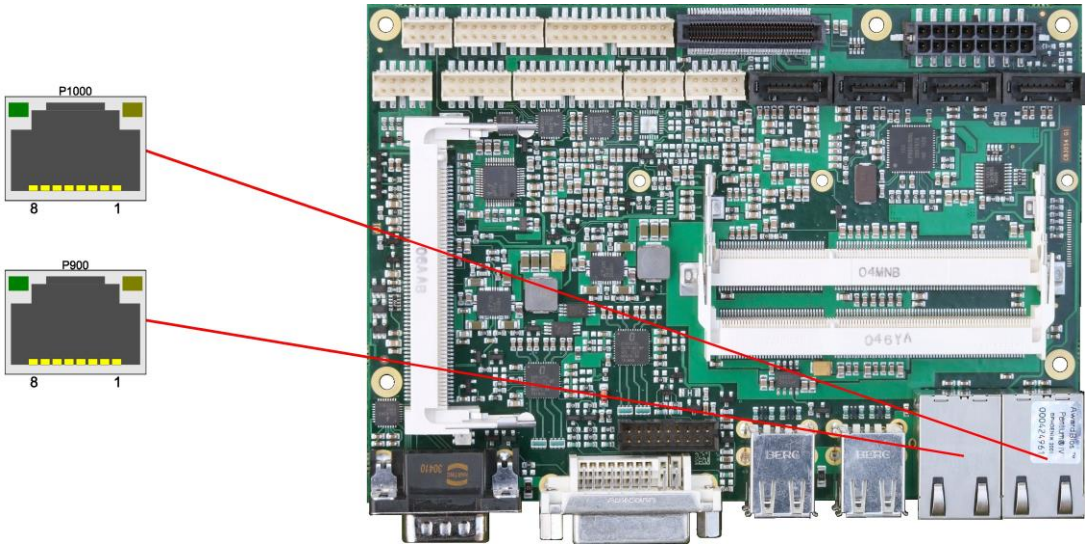
Description	Name	Pin		Name	Description
5 volt for USB5	VCC	1	9	VCC	5 volt for USB6
minus channel USB5	USB5-	2	10	USB6-	minus channel USB6
plus channel USB5	USB5+	3	11	USB6+	plus channel USB6
ground	GND	4	12	GND	ground
ground	GND	5	13	GND	ground
plus channel USB7	USB7+	6	14	USB8+	plus channel USB8
minus channel USB7	USB7-	7	15	USB8-	minus channel USB8
5 volt for USB7	VCC	8	16	VCC	5 volt for USB8

Pinout USB 9/10

Description	Name	Pin		Name	Description
5 volt for USB9	VCC	1	5	VCC	5 volt for USB10
minus channel USB9	USB9-	2	6	USB10-	minus channel USB10
plus channel USB9	USB9+	3	7	USB10+	plus channel USB10
ground	GND	4	8	GND	ground

3.10 LAN

The module has two LAN interfaces both of which support 10BaseT, 100BaseT, and 1000BaseT compatible net components with automatic bandwidth selection. Controller chips are Intel® 82567 (PHY, LAN1) and 82574L (MAC/PHY, LAN2). Auto-cross and auto-negotiate functionality is available as is PXE, RPL and WOL.

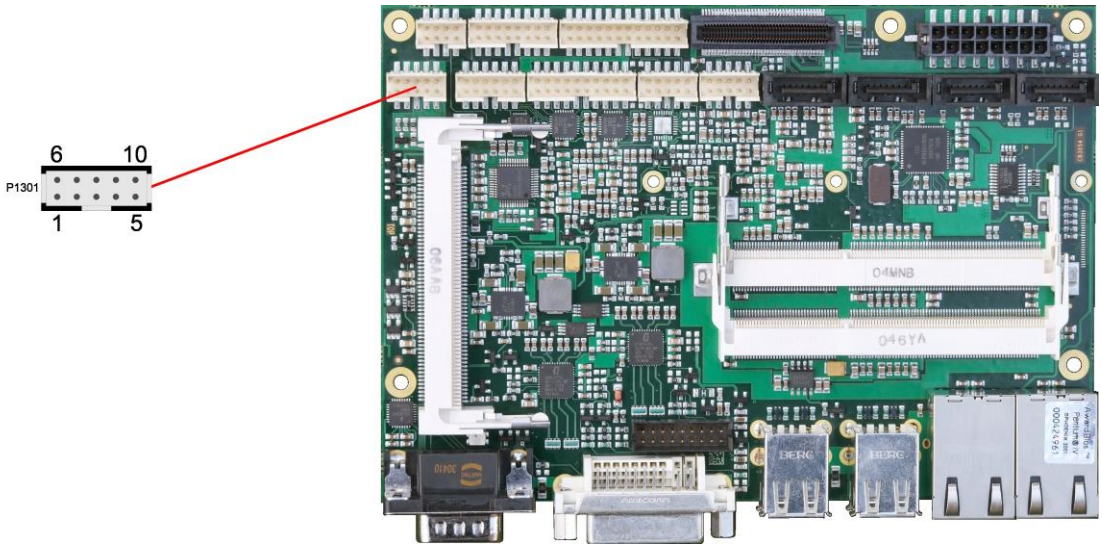


Pinout LAN 10/100/1000:

Pin	Name	Description
1	LAN-0	LAN channel 0 plus
2	LAN-0#	LAN channel 0 minus
3	LAN-1	LAN channel 1 plus
4	LAN-2	LAN channel 2 plus
5	LAN-2#	LAN channel 2 minus
6	LAN-1#	LAN channel 1 minus
7	LAN-3	LAN channel 3 plus
8	LAN-3#	LAN channel 3 minus

3.11 Audio

Audio input and output functions can be accessed via a 2x5 pin connector (FCI 98424-G52-10LF, mating connector FCI 90311-010LF). There are two ways to use this connector. Default functionality is the familiar audio in, audio out, and microphone. OS dependent device drivers can switch these signals to support a 5.1 output; thus in this mode no audio input signals are available.
Signals "SPDIFI" and "SPDIFO" provide digital input and output. If a transformation to a coaxial or optical connector is necessary this must be performed externally.

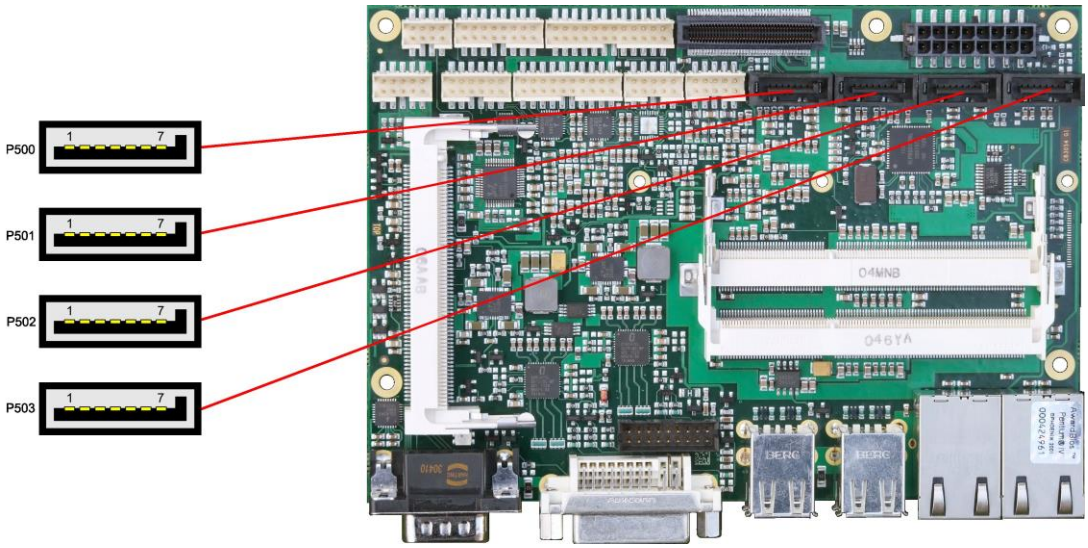


Pinout audio 2x5 pin connector:

Description	Name	Pin		Name	Description
digital output SPDIF	SPDIFO	1	6	3.3V	3.3 volt supply
digital input SPDIF	SPDIFI	2	7	S_AGND	analog ground sound
sound output right / front output right	LOUT_R / FRONT_R	3	8	LOUT_L / FRONT_L	sound output left / front output left
AUX input right / rear output right	AUXA_R / REAR_R	4	9	AUXA_L / REAR_L	AUX input left / rear output left
microphone input 1 / center output	MIC1 / CENTER	5	10	MIC2 / LFE	microphone input 2 / LFE output

3.12 SATA Interfaces

The CB3054 provides four SATA interfaces allowing transfer rates of up to 3 Gb/s. These interfaces are made available via two 7 pin connectors. RAID 0/1/5/10 is available.
The required settings are made in the BIOS setup.

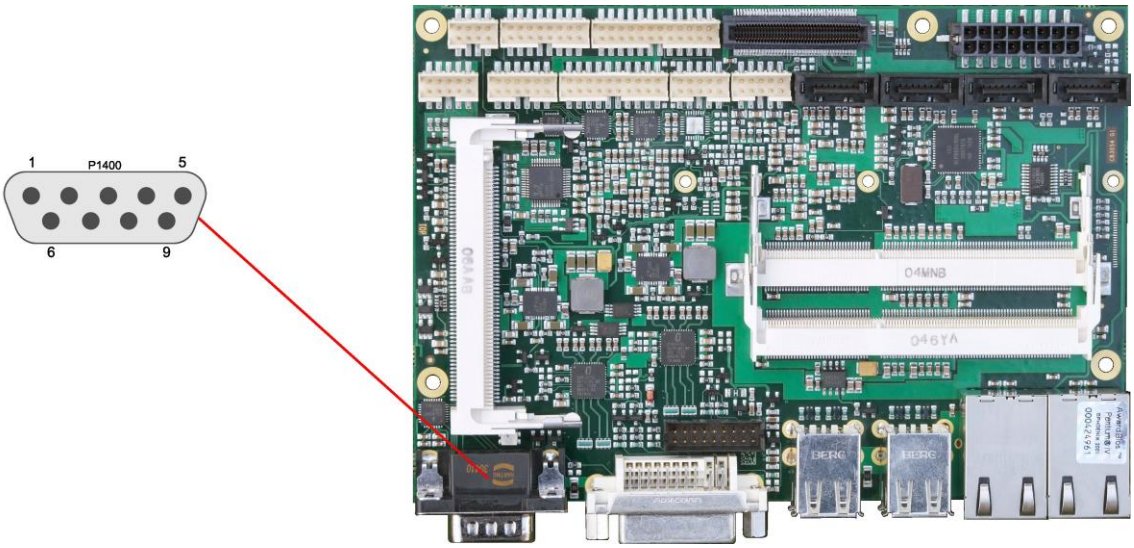


Pinout SATA:

Pin	Name	Description
1	GND	ground
2	SATATX	SATA transmit +
3	SATATX#	SATA transmit -
4	GND	ground
5	SATARX	SATA receive -
6	SATARX#	SATA receive +
7	GND	ground

3.13 Serial Interface COM1

The serial interface COM1 is made available via a 9-pin standard DSUB-connector (male, e.g. Foxconn DM10152-H5W3-4F). Signal level is RS232.
The port address and the interrupt are set via the BIOS setup.

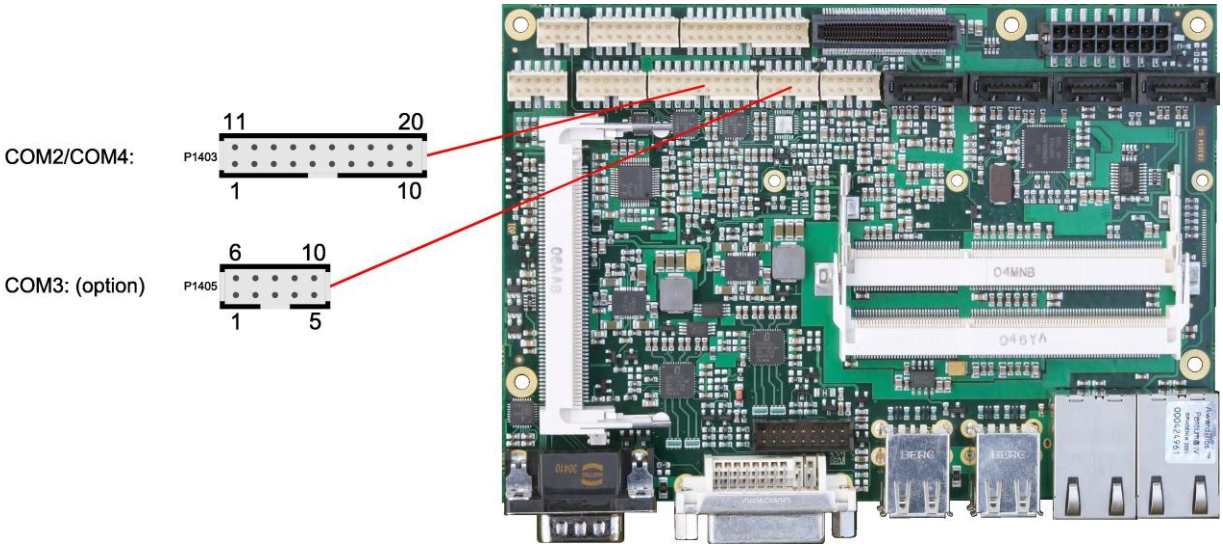


Pinout serial port (DSUB connector):

Description	Name	Pin		Name	Description
data carrier detect	DCD	1	6	DSR	data set ready
receive data	RXD	2	7	RTS	request to send
transmit data	TXD	3	8	CTS	clear to send
data terminal ready	DTR	4	9	RI	ring indicator
ground	GND	5			

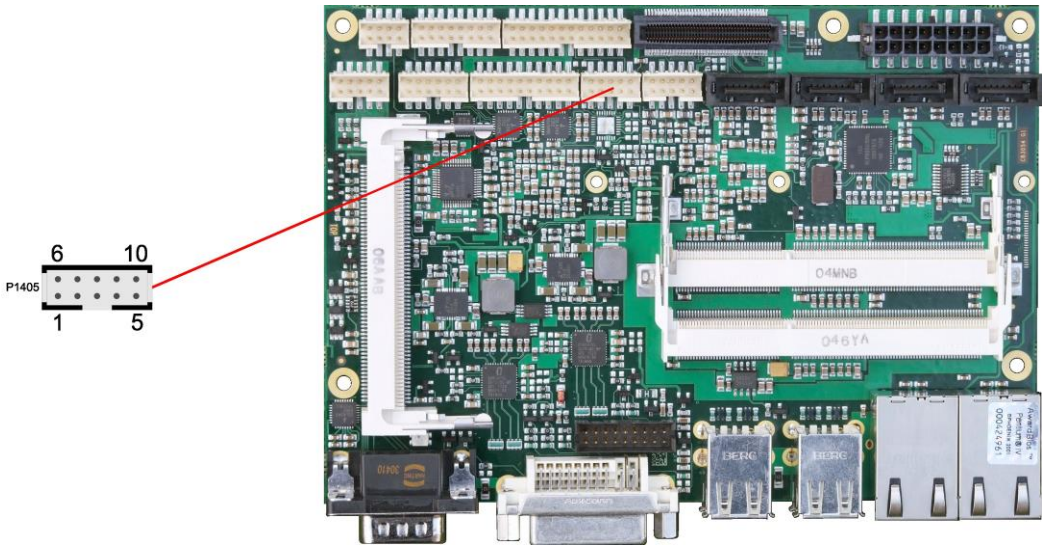
3.14 Serial Ports COM2 through COM4

There are three more serial interfaces on the board. Of these, COM3 is available through the power connector (cf. p. 18), or, as an option, through a 2x5pin connector (FCI 98424-G52-10LF). COM2 and COM4 and made available via a 2x10 pin connector (FCI 98424-G52-20LF). Signal level is RS232. The port address and the interrupt are set via the BIOS setup.



Description	Name	Pin		Name	Description
data carrier detect COM2	DCDB	1	11	DSRB	data set ready COM2
receive data COM2	RXDB	2	12	RTSB	request to send COM2
transmit data COM2	TXDB	3	13	CTSB	clear to send COM2
data terminal ready COM2	DTRB	4	14	RIB	ring indicator COM2
ground	GND	5	15	SVCC	5 volt supply
data carrier detect COM4	DCDD	6	16	DSRD	data set ready COM4
receive data COM4	RXDD	7	17	RTSD	request to send COM4
transmit data COM4	TXDD	8	18	CTSD	clear to send COM4
data terminal ready COM4	DTRD	9	19	RID	ring indicator COM4
ground	GND	10	20	SVCC	5 volt supply

When the module is ordered in standard configuration, the 2x5pin connector offers mouse and keyboard signals.

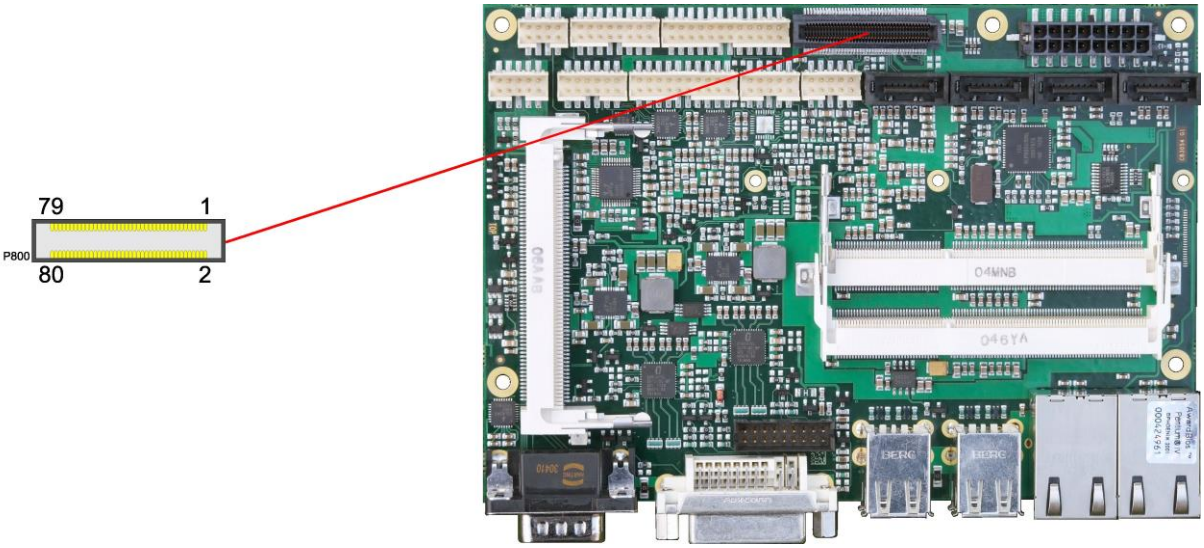


Alternative pinout of COM-connector:

Description	Name	Pin		Name	Description
keyboard clock	KCLK	1	6	MCLK	mouse clock
keyboard data	KDAT	2	7	MDAT	mouse data
reserved	N/C	3	8	N/C	reserved
reserved	N/C	4	9	N/C	reserved
ground	GND	5	10	3.3V	3.3 volt supply

3.15 PCI-Express

The CB3054 offers a 2x40pin custom connector for the PCI-Express bus. You can connect one PCIe4x device here. Alternatively, up to four PCIe1x devices can be connected. Adapter cards featuring standard PCIe sockets or a PCIe Mini Card connector are available. Please contact your sales representative for these cards.



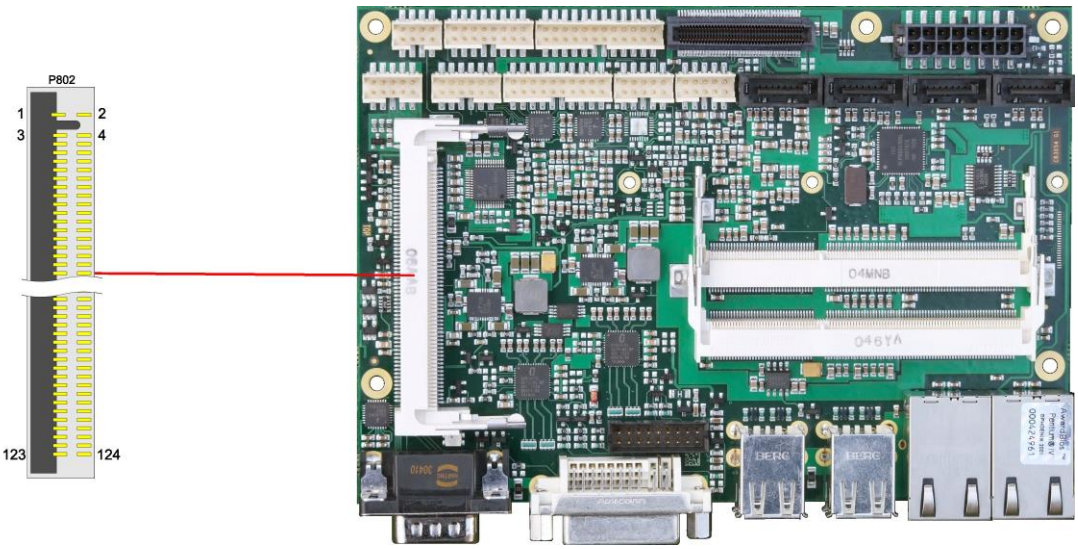
Pinout 2x40 pin connector PCIe:

Description	Name	Pin		Name	Description
3.3 volt supply	3.3V	1	2	12V	12 volt supply
3.3 volt stand-by	S3.3V	3	4	SMBCLK1	SMB clock slot 1
PCIe reset	PLTPCIE#	5	6	SMBDAT1	SMB dat slot 1
link reactivation	PEWAKE#	7	8	GND	ground
ground	GND	9	10	PECLK0	PCIe clock 0 +
transmit lane 1 +	PET1	11	12	PECLK0#	PCIe clock 0 -
transmit lane 1 -	PET1#	13	14	GND	ground
ground	GND	15	16	PER1	receive lane 1 +
clock enable 1	PE1CLKEN#	17	18	PER1#	receive lane 1 -
ground	GND	19	20	GND	ground
3.3 volt supply	3.3V	21	22	12V	12 volt supply
3.3 volt stand-by	S3.3V	23	24	SMBCLK2	SMB clock slot 2
PCIe reset	PLTPCIE#	25	26	SMBDAT2	SMB dat slot 2
link reactivation	PEWAKE#	27	28	GND	ground
ground	GND	29	30	PECLK1	PCIe clock 1 +
transmit lane 2 +	PET2	31	32	PECLK1#	PCIe clock 1 -
transmit lane 2 -	PET2#	33	34	GND	ground
ground	GND	35	36	PER2	receive lane 2 +
clock enable 2	PE2CLKEN#	37	38	PER2#	receive lane 2 -
ground	GND	39	40	GND	ground
3.3 volt supply	3.3V	41	42	12V	12 volt supply
3.3 volt stand-by	S3.3V	43	44	SMBCLK3	SMB clock slot 3
PCIe reset	PLTPCIE#	45	46	SMBDAT4	SMB dat slot 3
link reactivation	PEWAKE#	47	48	GND	ground
ground	GND	49	50	PECLK2	PCIe clock 2 +
transmit lane 3 +	PET3	51	52	PECLK2#	PCIe clock 2 -
transmit lane 3 -	PET3#	53	54	GND	ground

Description	Name	Pin		Name	Description
ground	GND	55	56	PER3	receive lane 3 +
clock enable 3	PE3CLKEN#	57	58	PER3#	receive lane 3 -
ground	GND	59	60	GND	ground
3.3 volt supply	3.3V	61	62	12V	12 volt supply
3.3 volt stand-by	S3.3V	63	64	SMBCLK4	SMB clock slot 4
PCIe reset	PLTPCIE#	65	66	SMBDAT4	SMB dat slot 4
link reactivation	PEWAKE#	67	68	GND	ground
ground	GND	69	70	PECLK3	PCIe clock 3 +
transmit lane 4 +	PET4	71	72	PECLK3#	PCIe clock 3 -
transmit lane 4 -	PET4#	73	74	GND	ground
ground	GND	75	76	PER4	receive lane 4 +
clock enable 4	PE3CLKEN#	77	78	PER4#	receive lane 4 -
PCIe configure x1/x4	PECONF#	79	80	GND	ground

3.16 Mini-PCI

The CB3054 allows you to add expansion cards complying to the Mini-PCI standard (type III). One such card can be inserted into the Mini-PCI slot available on the board.

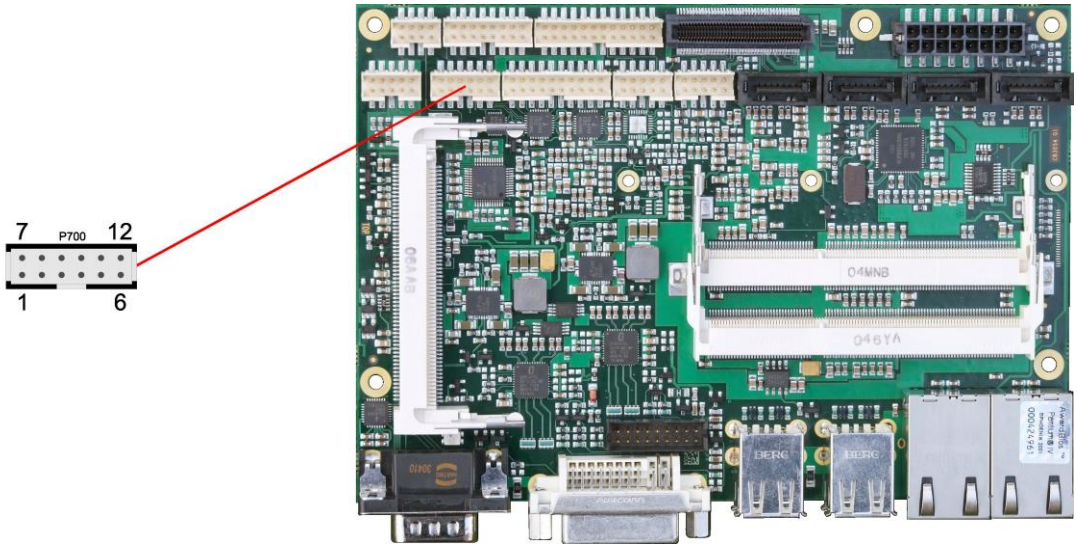


Description	Name	Pin		Name	Description
reserved	N/C	1	2	N/C	reserved
reserved	N/C	3	4	N/C	reserved
reserved	N/C	5	6	N/C	reserved
reserved	N/C	7	8	N/C	reserved
reserved	N/C	9	10	N/C	reserved
reserved	N/C	11	12	N/C	reserved
reserved	N/C	13	14	N/C	reserved
reserved	N/C	15	16	N/C	reserved
interrupt B	INTB#	17	18	VCC	5 volt supply
3.3 volt supply	3.3V	19	20	INTA#	interrupt A
serial interrupt (legacy)	SERIRQ	21	22	N/C	reserved
ground	GND	23	24	S3.3V	3.3 volt supply
PCI clock	PCLK	25	26	PRST#	reset
ground	GND	27	28	3.3V	3.3 volt supply
PCI request	REQ#	29	30	GNT#	PCI grant
3.3 volt supply	3.3V	31	32	GND	ground
address/data 31	AD31	33	34	PME#	power management event
address/data 29	AD29	35	36	N/C	reserved
ground	GND	37	38	AD30	address/data 30
address/data 27	AD27	39	40	3.3V	3.3 volt supply
address/data 25	AD25	41	42	AD28	address/data 28
interrupt C	INTC#	43	44	AD26	address/data 26
bus cmd/byte enables 3	CBE3#	45	46	AD24	address/data 24
address/data 23	AD23	47	48	IDSEL	init device select
ground	GND	49	50	GND	ground
address/data 21	AD21	51	52	AD22	address/data 22
address/data 19	AD19	53	54	AD20	address/data 20
ground	GND	55	56	PAR	parity
address/data 17	AD17	57	58	AD18	address/data 18

Description	Name	Pin		Name	Description
bus cmd/byte enables 2	CBE2#	59	60	AD16	address/data 16
initiator ready	IRDY#	61	62	GND	ground
3.3 volt supply	3.3V	63	64	FRAME#	cycle frame
clock running	CLKRUN#	65	66	TRDY#	target ready
system error	SERR#	67	68	STOP#	stop request by target
ground	GND	69	70	3.3V	3.3 volt supply
parity error	PERR#	71	72	DEVSEL#	device select
bus cmd/byte enables 1	CBE1#	73	74	GND	ground
address/data 14	AD14	75	76	AD15	address/data 15
ground	GND	77	78	AD13	address/data 13
address/data 12	AD12	79	80	AD11	address/data 11
address/data 10	AD10	81	82	GND	ground
ground	GND	83	84	AD9	address/data 9
address/data 8	AD8	85	86	CBE0#	bus cmd/byte enables 0
address/data 7	AD7	87	88	3.3V	3.3 volt supply
3.3 volt supply	3.3V	89	90	AD6	address/data 6
address/data 5	AD5	91	92	AD4	address/data 4
interrupt D	INTD#	93	94	AD2	address/data 2
address/data 3	AD3	95	96	AD0	address/data 0
5 volt supply	VCC	97	98	N/C	reserved
address/data 1	AD1	99	100	N/C	reserved
ground	GND	101	102	GND	ground
reserved	N/C	103	104	GND	ground
reserved	N/C	105	106	N/C	reserved
reserved	N/C	107	108	N/C	reserved
reserved	N/C	109	110	N/C	reserved
reserved	N/C	111	112	N/C	reserved
reserved	N/C	113	114	GND	ground
reserved	N/C	115	116	N/C	reserved
reserved	N/C	117	118	N/C	reserved
reserved	N/C	119	120	N/C	reserved
lock	PLOCK#	121	122	N/C	reserved
reserved	N/C	123	124	S3.3V	3.3 volt supply

3.17 GPIO

The General Purpose Input/Output interface is made available through a 2x6 pin connector (FCI 98424-G52-12LF, mating connector FCI 90311-012LF). To make use of this interface the GPIO chip (PCA9535BS) must be programmed accordingly. Please refer to your distributor for information on available software support.

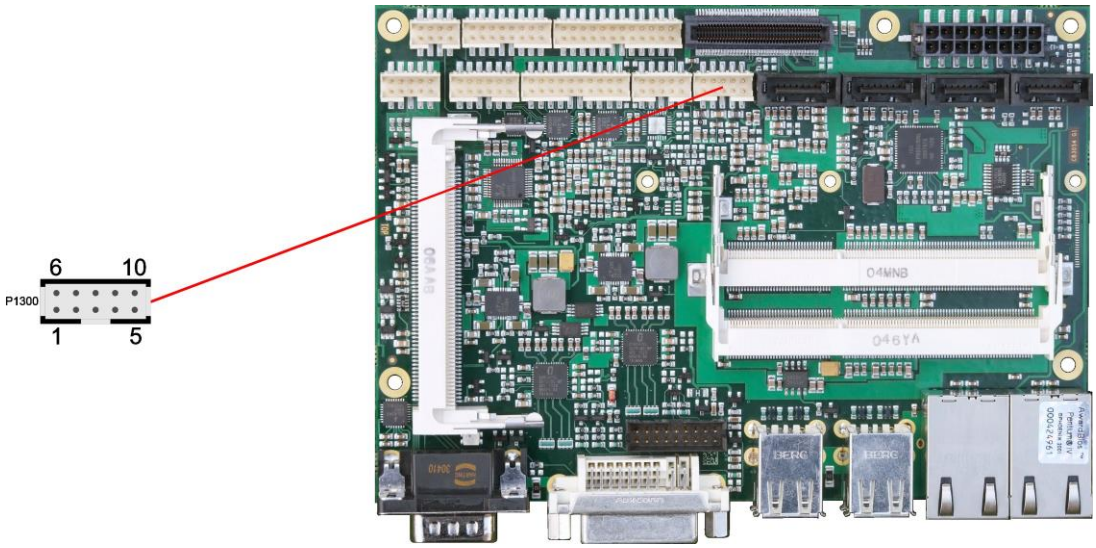


Pinout GPIO connector:

Description	Name	Pin		Name	Description
5 volt supply	VCC	1	7	VCC	5 volt supply
GP input/output 10	GPIO10	2	8	GPIO14	GP input/output 14
GP input/output 11	GPIO11	3	9	GPIO15	GP input/output 15
GP input/output 12	GPIO12	4	10	GPIO16	GP input/output 16
GP input/output 13	GPIO13	5	11	GPIO17	GP input/output 17
ground	GND	6	12	GND	ground

3.18 Fan Connectors

Three external fans (12V) can be connected to the board using a 2x5pin connector (FCI 98424-G52-10LF, mating connector FCI 90311-010LF). Monitoring signals are available. For the monitoring to work the fans must provide a corresponding speed signal.



Pinout fan connector:

Description	Name	Pin		Name	Description
ground	GND	1	6	GND	ground
12V regulated fan 1	FANON1	2	7	FANON2	12V regulated fan 2
monitoring signal fan 1	FANCTL1	3	8	FANCTL2	monitoring signal fan 2
12V regulated fan 3	FANON3	4	9	FANCTL3	monitoring signal fan 3
ground	GND	5	10	GND	ground

4 BIOS Settings

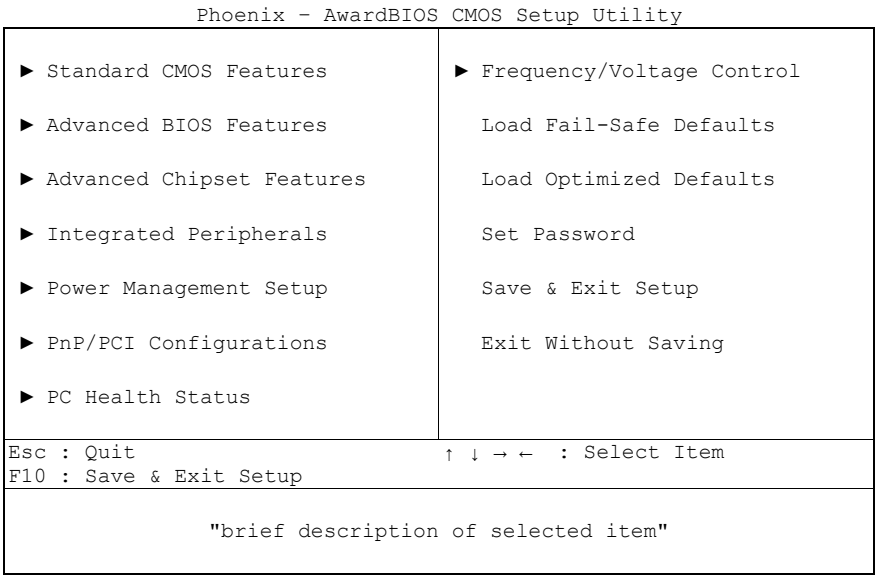
4.1 Remarks for Setup Use

In a setup page, standard values for its setup entries can be loaded. Fail-safe defaults are loaded with F6 and optimized defaults are loaded with F7. These standard values are independent of the fact that a board has successfully booted with a setup setting before.
This is different if these defaults are called from the Top Menu. Once a setup setting was saved, which subsequently leads to a successful boot process, those values are loaded as default for all setup items afterwards.
See also the chapters “Load Fail-Safe Defaults" (5.10) and “Load Optimized Defaults” (5.11).

NOTE

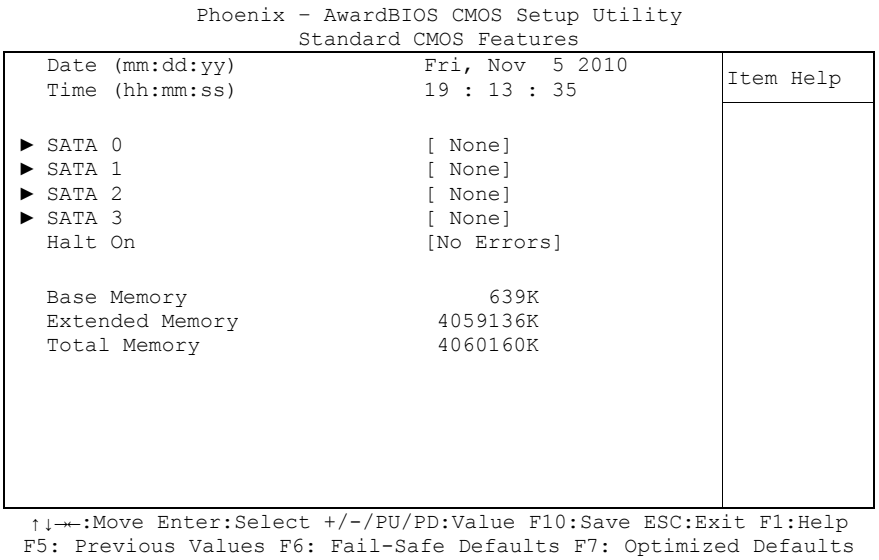
BIOS features and setup options are subject to change without notice. The settings displayed in the screenshots on the following pages are meant to be examples only. They do not represent the recommended settings or the default settings. Determination of the appropriate settings is dependent upon the particular application scenario in which the board is used.

4.2 Top Level Menu



The sign „►“ in front of an item means that there is a sub menu.
The „x“ sign in front of an item means, that the item is disabled but can be enabled by changing or selecting some other item (usually somewhere above the disabled item on the same screen).
Use the arrow buttons to navigate from one item to another. For selecting an item press Enter which will open either a sub menu or a dialog screen.

4.3 Standard CMOS Features



- ✓ **Date (mm:dd:yy)**
  Options: mm: month
  dd: day
  yy: year

- ✓ **Time (hh:mm:ss)**
  Options: hh: hours
  mm: minutes
  ss: seconds

- ✓ **SATA 1**
  Sub menu: see "SATA channels" (page 42)

- ✓ **SATA 2**
  Sub menu: see "SATA channels" (page 42)

- ✓ **SATA 3**
  Sub menu: see "SATA channels" (page 42)

- ✓ **SATA 4**
  Sub menu: see "SATA channels" (page 42)

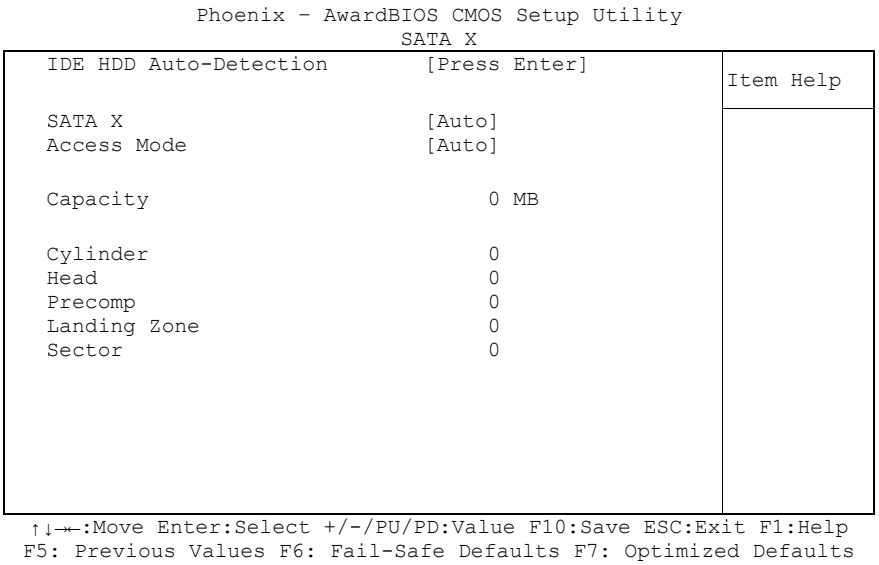
- ✓ **Halt On**
  Options: All Errors / No Errors / All, But Keyboard

- ✓ **Base Memory**
  Options: none

- ✓ **Extended Memory**
  Options: none

- ✓ **Total Memory**
  Options: none

4.3.1 SATA channels



- ✓ **SATA X**
  Options: None / Auto / Manual

- ✓ **Access Mode**
  Options: CHS / LBA / Large / Auto

- ✓ **Cylinder**
  Options: none

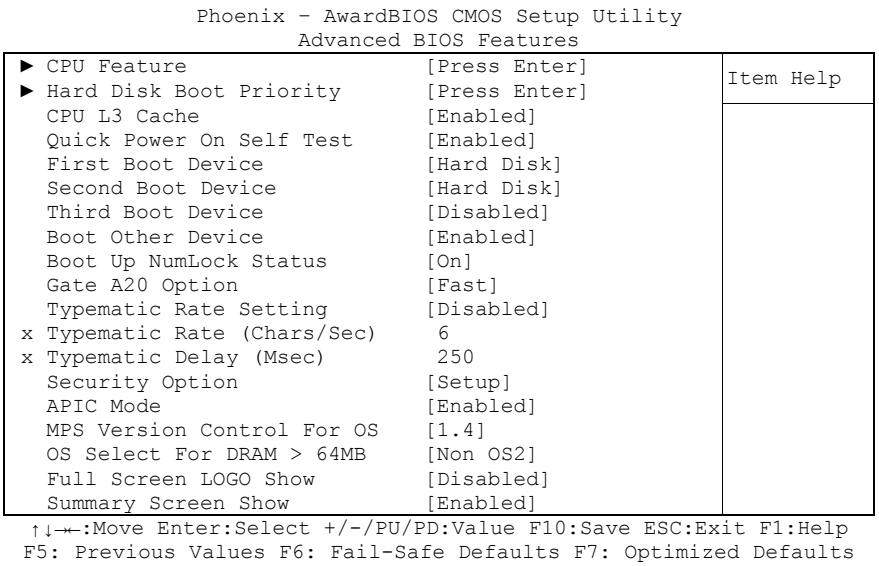
- ✓ **Head**
  Options: none

- ✓ **Precomp**
  Options: none

- ✓ **Landing Zone**
  Options: none

- ✓ **Sector**
  Options: none

4.4 Advanced BIOS Features



- ✓ **CPU Feature**
  Sub menu: see "CPU Feature" (page 45)

- ✓ **Hard Disk Boot Priority**
  Sub menu: see "Hard Disk Boot Priority" (page 46)

- ✓ **CPU L3 Cache**
  Options: Enabled / Disabled

- ✓ **Quick Power On Self Test**
  Options: Enabled / Disabled

- ✓ **First Boot Device**
  Options: LS120 / Hard Disk / CDROM / USB Device / ZIP100 / USB-FDD / USB-ZIP / Legacy LAN / IBA GE Slot 00C8 / Disabled

- ✓ **Second Boot Device**
  Options: LS120 / Hard Disk / CDROM / USB Device / ZIP100 / USB-FDD / USB-ZIP / Legacy LAN / IBA GE Slot 00C8 / Disabled

- ✓ **Third Boot Device**
  Options: LS120 / Hard Disk / CDROM / USB Device / ZIP100 / USB-FDD / USB-ZIP / Legacy LAN / IBA GE Slot 00C8 / Disabled

- ✓ **Boot Other Device**
  Options: Enabled / Disabled

- ✓ **Boot Up NumLock Status**
  Options: Off / On

- ✓ **Gate A20 Option**
  Options: Normal / Fast

- ✓ **Typematic Rate Setting**
  Options: Enabled / Disabled

- ✓ **Typematic Rate (Chars/Sec)**
  Options: 6 / 8 / 10 / 12 / 15 / 20 / 24 / 30

- ✓ **Typematic Delay (Msec)**
  Options: 250 / 500 / 750 / 1000

- ✓ **Security Option**
  Options: Setup / System

- ✓ **APIC Mode**
  Options: Enabled / Disabled

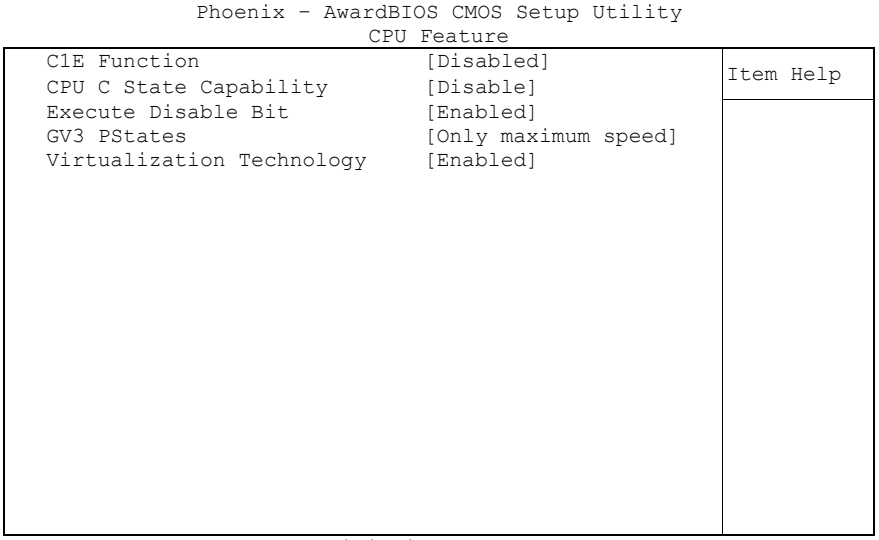
- ✓ **MPS Version Control For OS**
  Options: 1.1 / 1.4

- ✓ **OS Select For DRAM > 64MB**
  Options: Non-OS2 / OS2

- ✓ **Full Screen LOGO Show**
  Options: Enabled / Disabled

- ✓ **Summary Screen Show**
  Options: Enabled / Disabled

4.4.1 CPU Feature



- ✓ **C1E Function**
  Options: Auto / Disabled

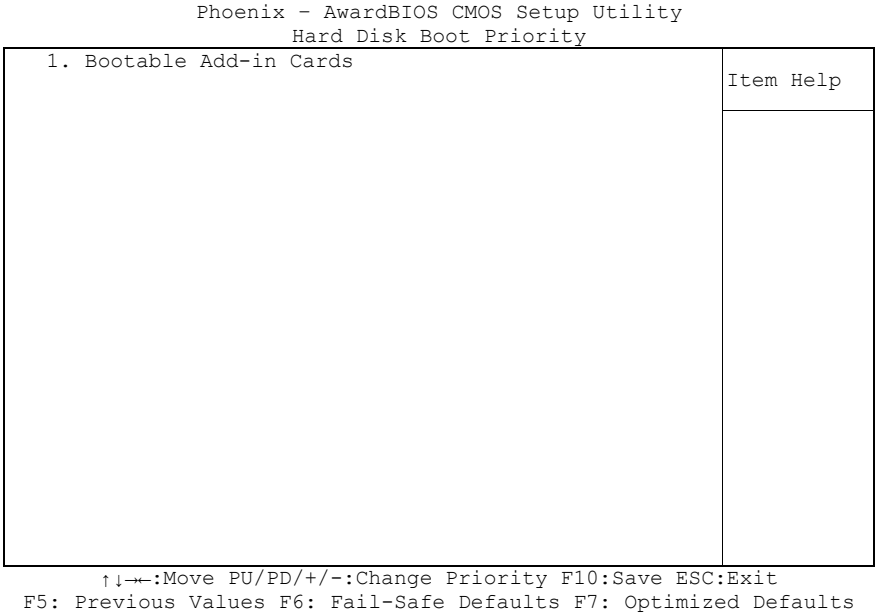
- ✓ **CPU C State Capability**
  Options: Disabled / C2 / C3 / C4

- ✓ **Execute Disable Bit**
  Options: Enabled / Disabled

- ✓ **GV3 PStates**
  Options: Only maximum speed / All PStates

- ✓ **Virtualization Technology**
  Options: Enabled / Disabled

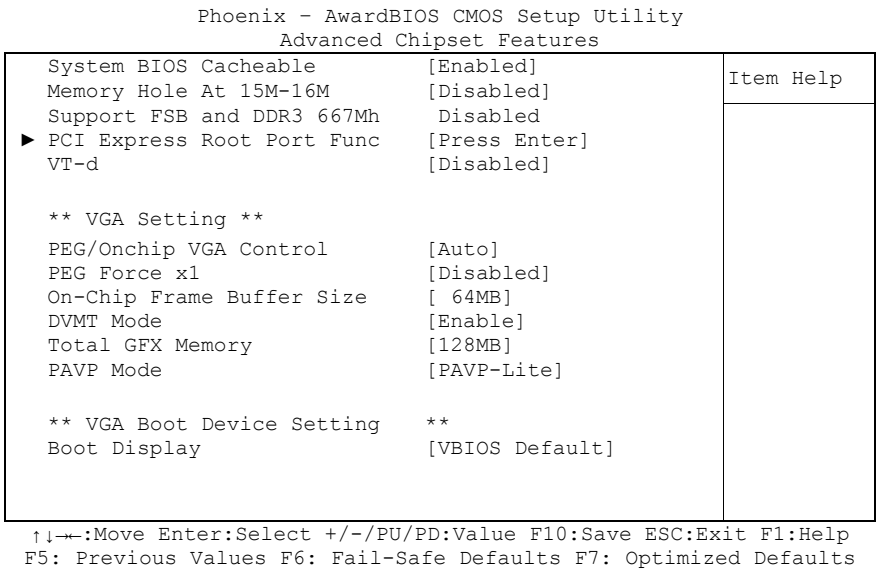
4.4.2 Hard Disk Boot Priority



✓ **[list of available devices]**
Options: this dialog allows you to set the order in which the available bootable devices shall be accessed for an attempt to boot.

✓ **Attention!**
in this sub menu the buttons <Page Up>, <Page Down>, <+> and <-> have a different function than in the rest of the setup: They serve to move the items of the list up or down.

4.5 Advanced Chipset Features



- ✓ **System BIOS Cacheable**
  Options: Enabled / Disabled

- ✓ **Memory Hole At 15M-16M**
  Options: Enabled / Disabled

- ✓ **Support FSB and DDR3 667Mhz**
  Options: none

- ✓ **PCI Express Root Port Func**
  Sub menu: see "PCI Express Root Port Function" (page 48)

- ✓ **VT-d**
  Options: Enabled / Disabled

- ✓ **PEG/Onchip VGA Control**
  Options: Onchip VGA / PEG Port / Auto

- ✓ **PEG Force X1**
  Options: Enabled / Disabled

- ✓ **On-Chip Frame Buffer Size**
  Options: 32MB / 64MB / 128MB

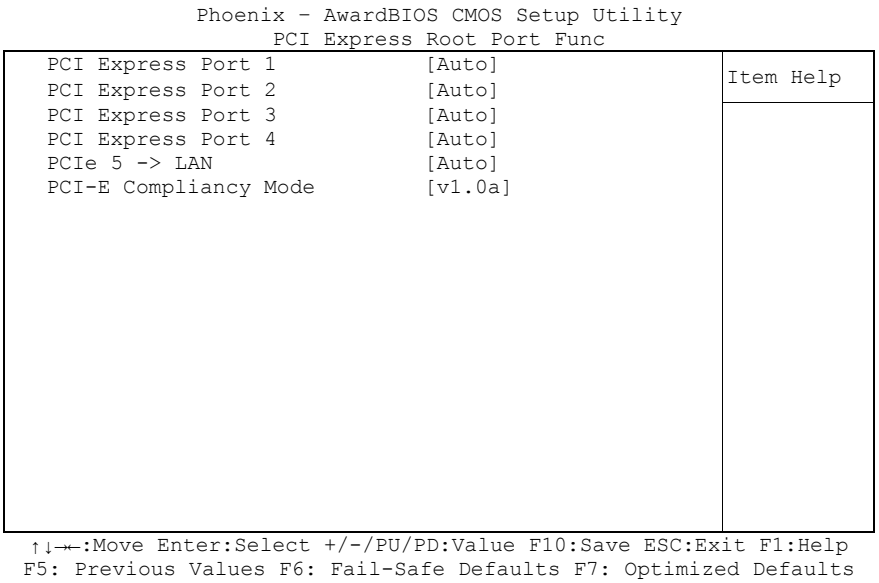
- ✓ **DVMT Mode**
  Options: Disable / Enable

- ✓ **Total GFX Memory**
  Options: 128MB / 256MB / MAX.

- ✓ **PAVP Mode**
  Options: Disable / PAVP-Lite / PAVP-High

- ✓ **Boot Display**
  Options: VBIOS Default / CRT / DVI / DVI intern / CRT+DVI

4.5.1 PCI Express Root Port Function



- ✓ **PCI Express Port 1**
  Options: Auto / Enabled / Disabled

- ✓ **PCI Express Port 2**
  Options: Auto / Enabled / Disabled

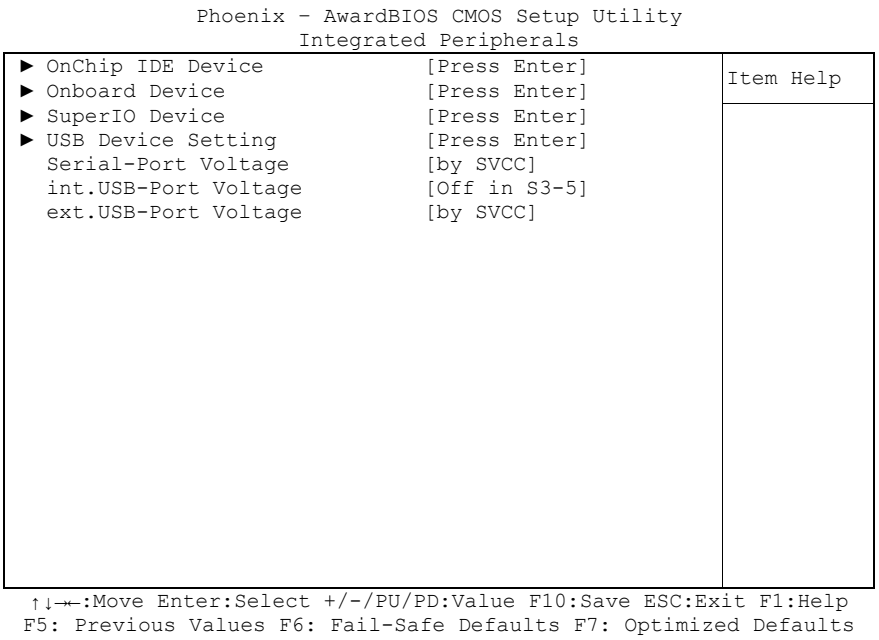
- ✓ **PCI Express Port 3**
  Options: Auto / Enabled / Disabled

- ✓ **PCI Express Port 4**
  Options: Auto / Enabled / Disabled

- ✓ **PCIe 5 -> LAN**
  Options: Auto / Enabled / Disabled

- ✓ **PCI-E Compliancy Mode**
  Options: v1.0a / v1.0

4.6 Integrated Peripherals



- ✓ **OnChip IDE Device**
  Sub menu: see "OnChip IDE Devices" (page 50)

- ✓ **Onboard Device**
  Sub menu: see "Onboard Devices" (page 52)

- ✓ **SuperIO Device**
  Sub menu: see "SuperIO Devices" (page 53)

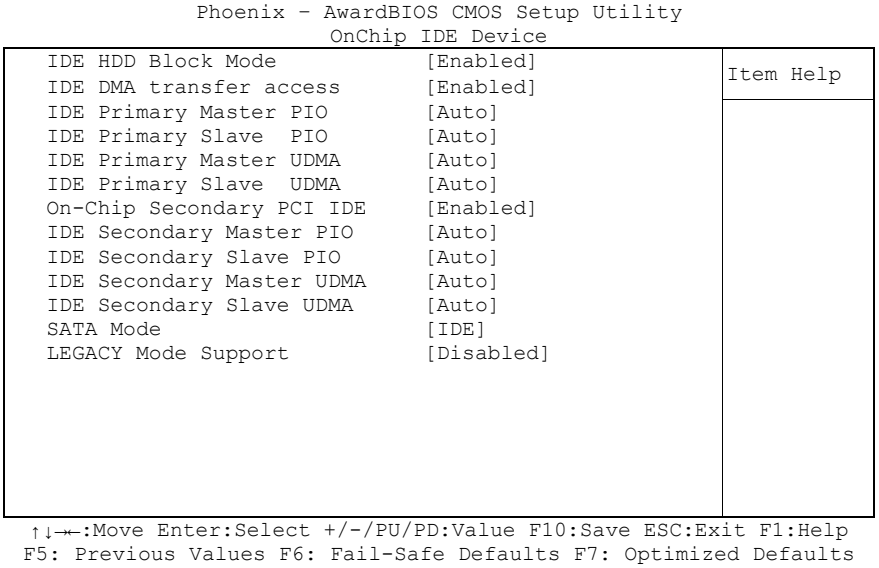
- ✓ **USB Device Setting**
  Sub menu: see "USB Device Setting" (page 54)

- ✓ **Serial-Port Voltage**
  Options: Off in S3-5 / by SVCC

- ✓ **int.USB-Port Voltage**
  Options: Off in S3-5 / by SVCC

- ✓ **ext.USB-Port Voltage**
  Options: Off in S3-5 / by SVCC

4.6.1 OnChip IDE Devices



- ✓ **IDE HDD Block Mode**
  Options: Enabled / Disabled

- ✓ **IDE DMA transfer access**
  Options: Enabled / Disabled

- ✓ **IDE Primary Master PIO**
  Options: Auto / Mode 0 / Mode 1 / Mode 2 / Mode 3 / Mode 4

- ✓ **IDE Primary Slave PIO**
  Options: Auto / Mode 0 / Mode 1 / Mode 2 / Mode 3 / Mode 4

- ✓ **IDE Primary Master UDMA**
  Options: Disabled / Auto

- ✓ **IDE Primary Slave UDMA**
  Options: Disabled / Auto

- ✓ **On-Chip Secondary PCI IDE**
  Options: Enabled / Disabled

- ✓ **IDE Secondary Master PIO**
  Options: Auto / Mode 0 / Mode 1 / Mode 2 / Mode 3 / Mode 4

- ✓ **IDE Secondary Slave PIO**
  Options: Auto / Mode 0 / Mode 1 / Mode 2 / Mode 3 / Mode 4

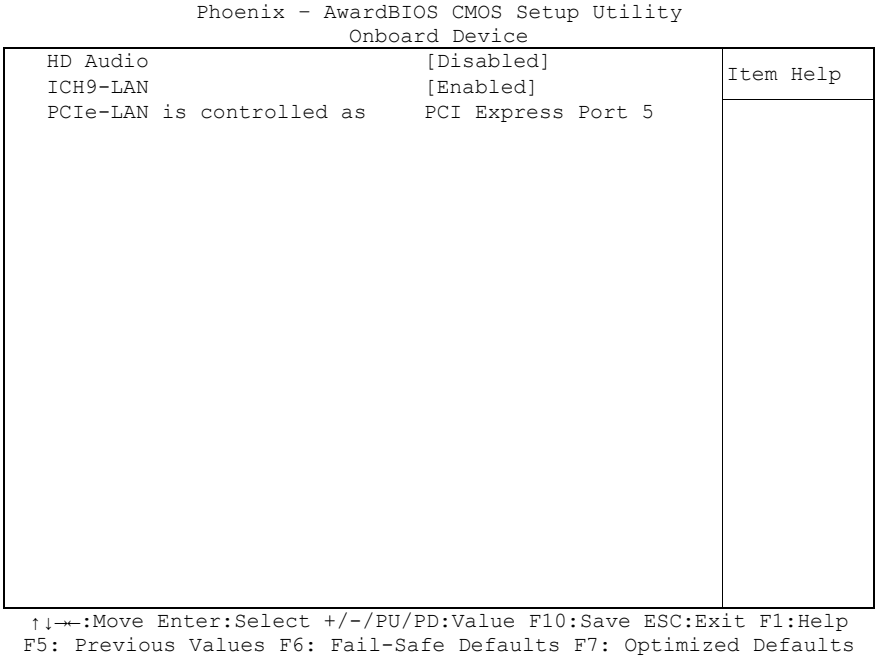
- ✓ **IDE Secondary Master UDMA**
  Options: Disabled / Auto

- ✓ **IDE Secondary Slave UDMA**
  Options: Disabled / Auto

- ✓ **SATA Mode**
  Options: IDE / RAID / AHCI

✓ **LEGACY Mode Support**
Options: Enabled / Disabled

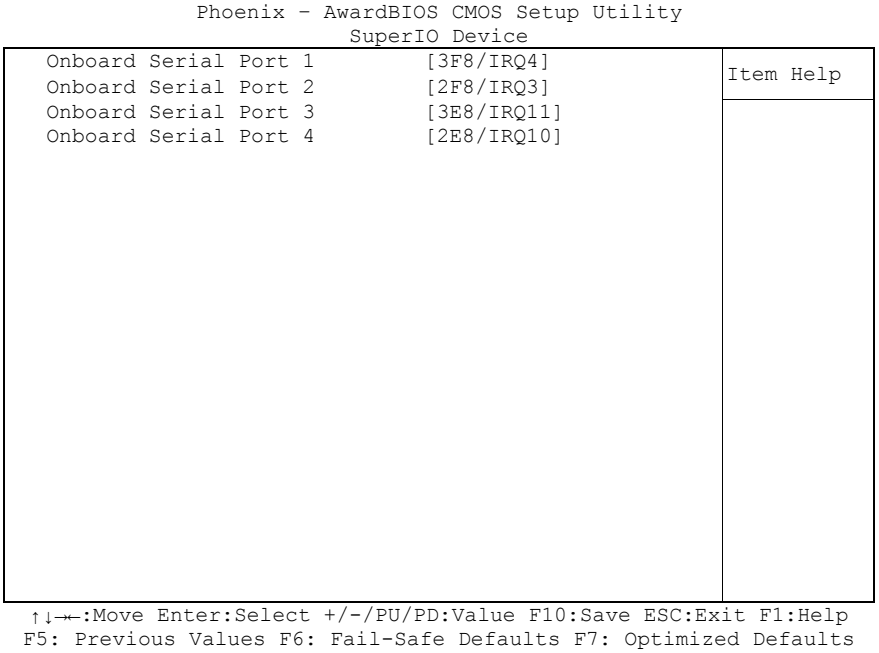
4.6.2 Onboard Devices



- ✓ **HD Audio**
  Options: Auto / Disabled

- ✓ **ICH9-LAN**
  Options: Enabled / Disabled

4.6.3 SuperIO Devices



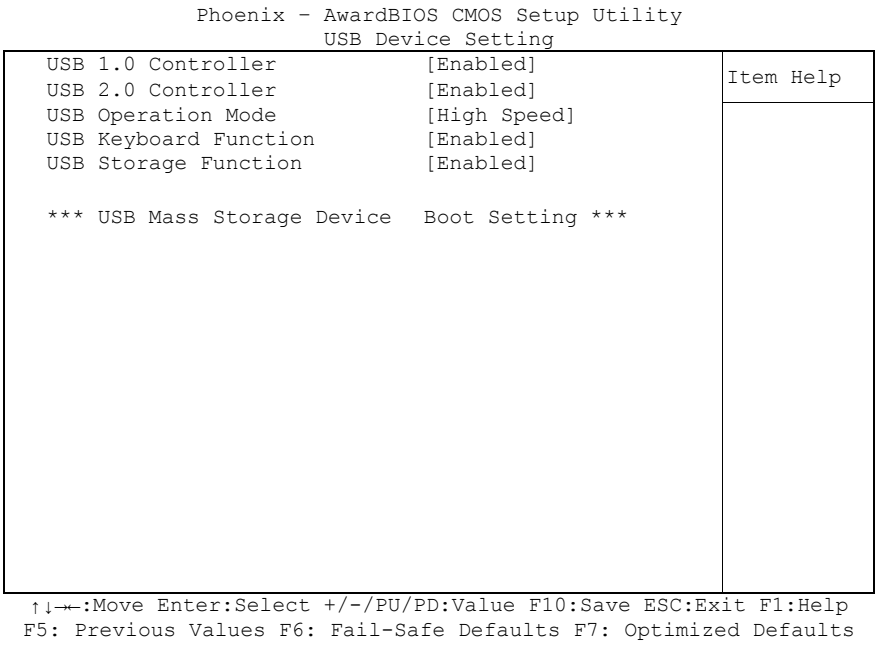
- ✓ **Onboard Serial Port 1**
  Options: Disabled / 3F8/IRQ4 / 2F8/IRQ3 / 3E8/IRQ4 / 2E8/IRQ3

- ✓ **Onboard Serial Port 2**
  Options: Disabled / 3F8/IRQ4 / 2F8/IRQ3 / 3E8/IRQ4 / 2E8/IRQ3

- ✓ **Onboard Serial Port 3**
  Options: Disabled / 3F8/IRQ11 / 2F8/IRQ11 / 3E8/IRQ11 / 2E8/IRQ11

- ✓ **Onboard Serial Port 4**
  Options: Disabled / 3F8/IRQ10 / 2F8/IRQ10 / 3E8/IRQ10 / 2E8/IRQ10

4.6.4 USB Device Setting



- ✓ **USB 1.0 Controller**
  Options: Enabled / Disabled

- ✓ **USB 2.0 Controller**
  Options: Enabled / Disabled

- ✓ **USB Operation Mode**
  Options: Full/Low Speed / High Speed

- ✓ **USB Keyboard Function**
  Options: Enabled / Disabled

- ✓ **USB Storage Function**
  Options: Enabled / Disabled

4.7 Power Management Setup

```
                    Phoenix – AwardBIOS CMOS Setup Utility
                          Power Management Setup
 ► PCI Express PM Function       [Press Enter]   |  Item Help
   ACPI Function                 [Enabled]       |
   ACPI Suspend Type             [S1(POS)]       |
 x Run VGABIOS if S3 Resume       Auto           |
   Power Management              [User Define]   |
   Video Off Method              [DPMS]          |
   Video Off in Suspend          [Yes]           |
   Suspend Type                  [Stop Grant]    |
   Modem Use IRQ                 [3]             |
   Suspend Mode                  [Disabled]      |
   HDD Power Down                [Disabled]      |
   Soft-Off by PWR-BTTN          [Instant-Off]   |
   PWRON After PWR-Fail          [On]            |
   Wake-Up by PCI card           [Disabled]      |
   Power On by Ring              [Disabled]      |
 x USB KB Wake-Up From S3       Disabled         |
   Resume by Alarm               [Disabled]      |
 x  Date(of Month) Alarm          0              |
 x  Time(hh:mm:ss)                0 : 0 : 0      |

   ** Reload Global Timer        Events **       |
   Primary IDE 0                 [Disabled]      |
   Primary IDE 1                 [Disabled]      |
   Secondary IDE 0               [Disabled]      |
   Secondary IDE 1               [Disabled]      |
   FDD,COM,LPT Port              [Disabled]      |
   PCI PIRQ[A-D]#                [Disabled]      |
   HPET Support                  [Enabled]       |
   HPET Mode                     [32-bit mode]   |
 ► Intel DTS Feature             [Press Enter]   |
  ↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
 F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults
```

- ✓ **PCI Express PM Function**
  Sub menu: see "PCI Express PM Function" (page 57)

- ✓ **ACPI function**
  Options: Enabled / Disabled

- ✓ **ACPI Suspend Type**
  Options: S1(POS) / S3(STR) / S1&S3

- ✓ **Run VGABIOS if S3 Resume**
  Options: Auto / Yes / No

- ✓ **Power Management**
  Options: User Define / Min Saving / Max Saving

- ✓ **Video Off Method**
  Options: Blank Screen / V/H SYNC+Blank / DPMS

- ✓ **Video Off In Suspend**
  Options: No / Yes

- ✓ **Suspend Type**
  Options: Stop Grant / PwrOn Suspend

- ✓ **MODEM Use IRQ**
  Options: NA / 3 / 4 / 5 / 7 / 9 / 10 / 11

- ✓ **Suspend Mode**
  Options: Disabled / 1 Min / 2 Min / 4 Min / 8 Min / 12 Min / 20 Min / 30 Min / 40 Min / 1 Hour

- ✓ **HDD Power Down**
  Options: Disabled / 1 Min ... 15 Min

- ✓ **Soft-Off by PWR-BTTN**
  Options: Instant-Off / Delay 4 Sec

- ✓ **PWRON After PWR-Fail**
  Options: Former Sts / On / Off

- ✓ **Wake Up by PCI Card**
  Options: Enabled / Disabled

- ✓ **Power-On by Ring**
  Options: Enabled / Disabled

- ✓ **USB KB Wake Up From S3**
  Options: Enabled / Disabled

- ✓ **Resume by Alarm**
  Options: Enabled / Disabled

- ✓ **Date(of Month) Alarm**
  Options: 1 / ... / 31

- ✓ **Time (hh:mm:ss) Alarm**
  Options: insert [hh], [mm] and [ss]

- ✓ **Primary IDE 0**
  Options: Enabled / Disabled

- ✓ **Primary IDE 1**
  Options: Enabled / Disabled

- ✓ **Secondary IDE 0**
  Options: Enabled / Disabled

- ✓ **Secondary IDE 1**
  Options: Enabled / Disabled

- ✓ **FDD,COM,LPT Port**
  Options: Enabled / Disabled

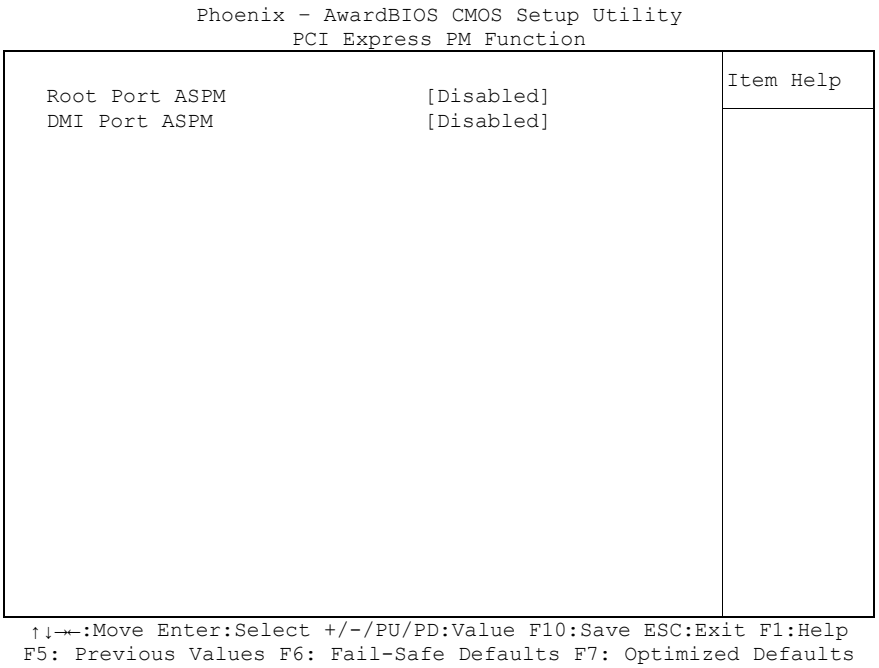
- ✓ **PCI PIRQ[A-D]#**
  Options: Enabled / Disabled

- ✓ **HPET Support**
  Options: Enabled / Disabled

- ✓ **HPET Mode**
  Options: 32-bit mode / 64-bit mode

- ✓ **Intel DTS Feature**
  Sub menu: see "Intel DTS Feature" (page 58)

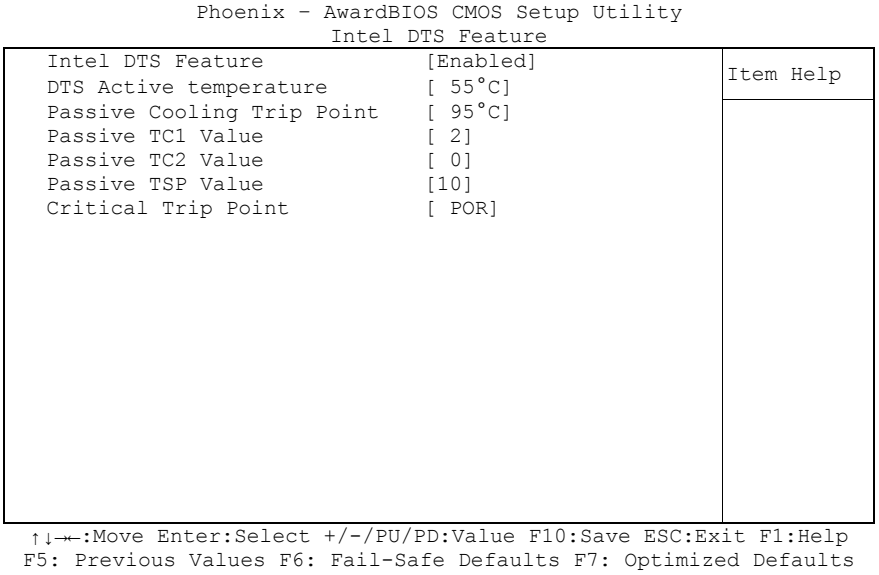
4.7.1 PCI Express PM Function



- ✓ **Root Port ASPM**
  Options: Disabled / L0s / L1 / L1/L0s

- ✓ **DMI Port ASPM**
  Options: Enabled / Disabled

4.7.2 Intel DTS Feature



- ✓ **Intel DTS Function**
  Options: Enabled / Disabled

- ✓ **DTS Active temperature**
  Options: 15°C / 23°C / 31°C / 39°C / 47°C / 55°C / 63°C / 71°C / 79°C / 87°C / 95°C / 103°C / 111°C / 119°C

- ✓ **Passive Cooling Trip Point**
  Options: 15°C / 23°C / 31°C / 39°C / 47°C / 55°C / 63°C / 71°C / 79°C / 87°C / 95°C / 103°C / 111°C / 119°C

- ✓ **Passive TC1 Value**
  Options: 0 / 1 / ... / 14 / 15

- ✓ **Passive TC2 Value**
  Options: 0 / 1 / ... / 14 / 15

- ✓ **Passive TSP Value**
  Options: 0 / 1 / ... / 14 / 15

- ✓ **Critical Trip Point**
  Options: POR / 15°C / 23°C / 31°C / 39°C / 47°C / 55°C / 63°C / 71°C / 79°C / 87°C / 95°C / 103°C / 111°C / 119°C / 127°C

4.8 PnP/PCI Configuration

```
                Phoenix – AwardBIOS CMOS Setup Utility
                      PNP/PCI Configurations
  Init Display First            [PCI Slot]          | Item Help
  Reset Configuration Data      [Disabled]          |
                                                    |
  Resources Controlled By       [Manual]            |
► IRQ Resources                 [Press Enter]       |
                                                    |
  PCI/VGA Palette Snoop         [Disabled]          |
  INT Pin 1 Assignment          [Auto]              |
  INT Pin 2 Assignment          [Auto]              |
  INT Pin 3 Assignment          [Auto]              |
  INT Pin 4 Assignment          [Auto]              |
  INT Pin 5 Assignment          [Auto]              |
  INT Pin 6 Assignment          [Auto]              |
  INT Pin 7 Assignment          [Auto]              |
  INT Pin 8 Assignment          [Auto]              |
                                                    |
  ** PCI Express relative       items **            |
  Maximum Payload Size          [128]               |
                                                    |
↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:Help
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults
```

- ✓ **Init Display First**
  Options: PCI Slot / Onboard

- ✓ **Reset Configuration Data**
  Options: Enabled / Disabled

- ✓ **Resources Controlled By**
  Options: Auto(ESCD) / Manual

- ✓ **IRQ Resources**
  Sub menu: see "IRQ Resources" (page 61)

- ✓ **PCI/VGA Palette Snoop**
  Options: Enabled / Disabled

- ✓ **INT Pin 1 Assignment**
  Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

- ✓ **INT Pin 2 Assignment**
  Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

- ✓ **INT Pin 3 Assignment**
  Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

- ✓ **INT Pin 4 Assignment**
  Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

- ✓ **INT Pin 5 Assignment**
  Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

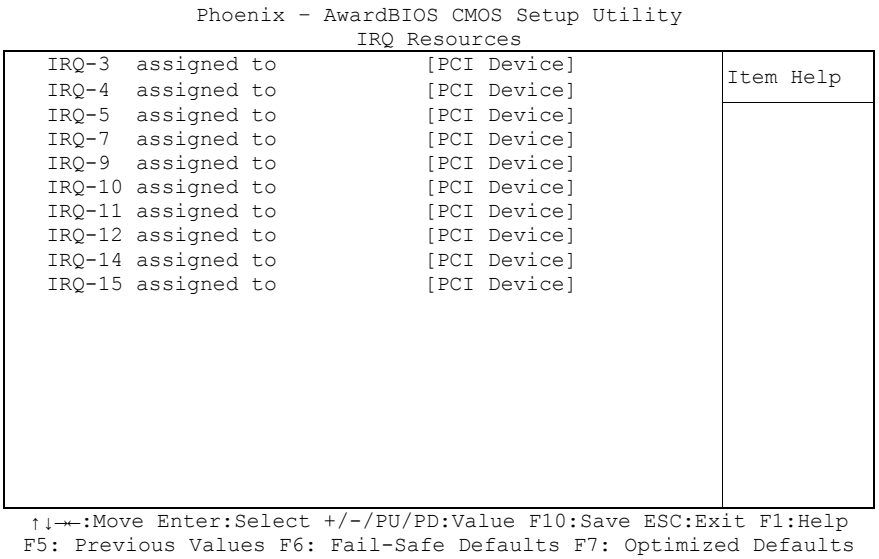
- ✓ **INT Pin 6 Assignment**
  Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

- ✓ **INT Pin 7 Assignment**
  Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

- ✓ **INT Pin 8 Assignment**
  Options: Auto / 3 / 4 / 5 / 7 / 9 / 10 / 11 / 12 / 14 / 15

- ✓ **Maximum Payload Size**
  Options: none

4.8.1 IRQ Resources



- ✓ **IRQ-3 assigned to**
  Options: PCI Device / Reserved

- ✓ **IRQ-4 assigned to**
  Options: PCI Device / Reserved

- ✓ **IRQ-5 assigned to**
  Options: PCI Device / Reserved

- ✓ **IRQ-7 assigned to**
  Options: PCI Device / Reserved

- ✓ **IRQ-9 assigned to**
  Options: PCI Device / Reserved

- ✓ **IRQ-10 assigned to**
  Options: PCI Device / Reserved

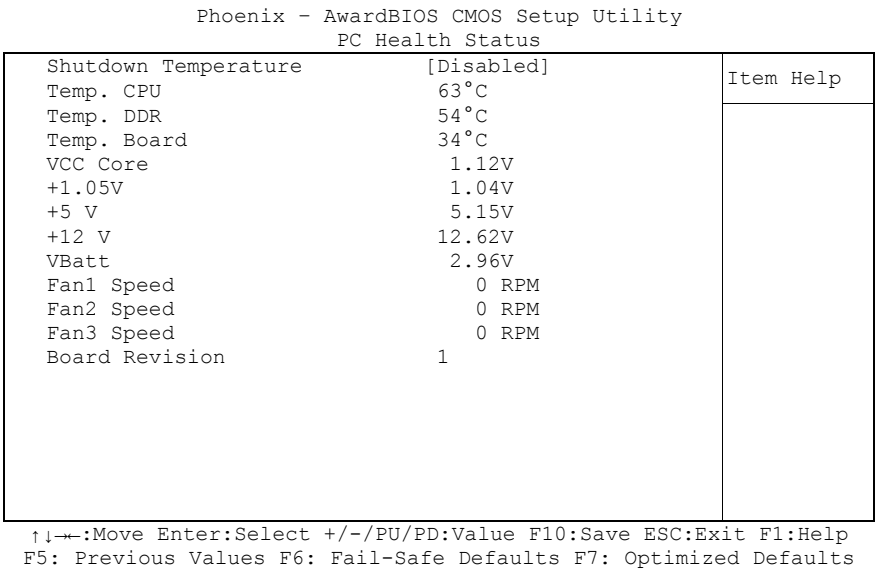
- ✓ **IRQ-11 assigned to**
  Options: PCI Device / Reserved

- ✓ **IRQ-12 assigned to**
  Options: PCI Device / Reserved

- ✓ **IRQ-14 assigned to**
  Options: PCI Device / Reserved

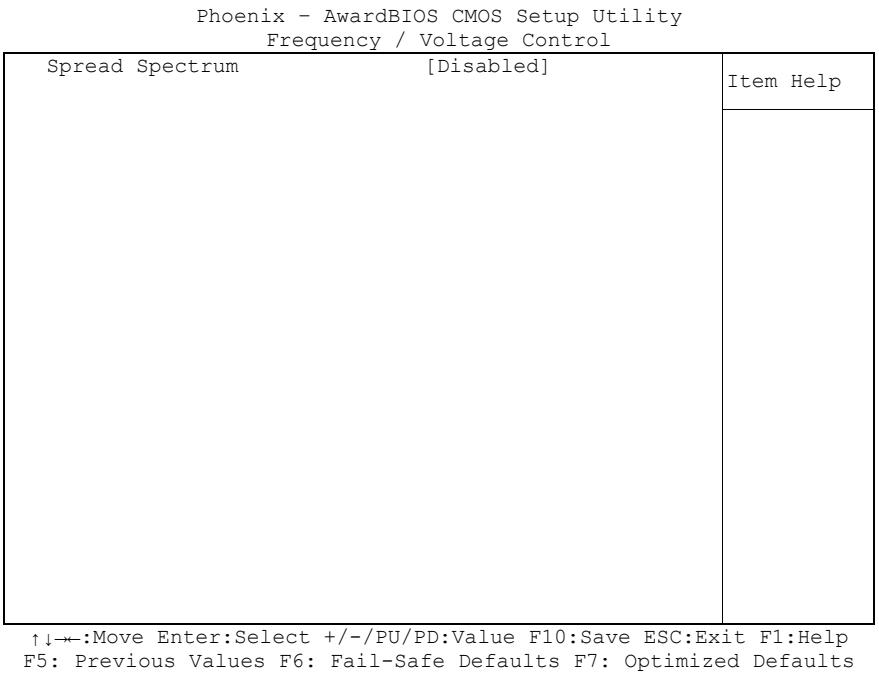
- ✓ **IRQ-15 assigned to**
  Options: PCI Device / Reserved

4.9 PC Health Status



- ✓ **Temp. CPU**
  Options: none
- ✓ **Temp. DDR**
  Options: none
- ✓ **Temp. Board**
  Options: none
- ✓ **VCC Core**
  Options: none
- ✓ **+1.05 V**
  Options: none
- ✓ **+5 V**
  Options: none
- ✓ **+12 V**
  Options: none
- ✓ **VBatt**
  Options: none
- ✓ **Fan1 Speed**
  Options: none
- ✓ **Fan2 Speed**
  Options: none
- ✓ **Fan3 Speed**
  Options: none
- ✓ **Board Revision**
  Options: none

4.10 Frequency/Voltage Control



✓ **Spread Spectrum**
Options: Enabled / Disabled

4.11 Load Fail-Safe Defaults

If this option is chosen, the last working setup is loaded from flash. Working means that the setup setting has already led to a successful boot process.
At the first setting of the BIOS setup, safe values are loaded which lets the board boot. This status is reached again, if the board is reprogrammed with the corresponding flash-program and the required parameters.

4.12 Load Optimized Defaults

This option applies like described under “Remarks for Setup Use” (5.1).
At first start of the BIOS, optimized values are loaded from the setup, which are supposed to make the board boot. This status is achieved again, if the board is reprogrammed using the flash program with the required parameters.

4.13 Set Password

Here you can enter a password to protect the BIOS settings against unauthorized changes. Use this option with care! Forgotten or lost passwords are a frequent problem.

4.14 Save & Exit Setup

Settings are saved and the board is restarted.

4.15 Exit Without Saving

This option leaves the setup without saving any changes.

5 BIOS update

If a BIOS update becomes necessary, the program “AWDFLASH.EXE” from Phoenix Technologies is used for this. It is important, that the program is started from a DOS environment without a virtual memory manager such as for example “EMM386.EXE”. In case such a memory manager is loaded, the program will stop with an error message.
The system must not be interrupted during the flash process, otherwise the update is stopped and the BIOS is destroyed afterwards.
The program should be started as follows:

```
awdflash [biosfilename] /sn /cc /cp
```

/sn	Do not save the current BIOS
/cc	Clear the CMOS
/cp	Clear the PnP information

The erasure of CMOS and PnP is strongly recommended. This ensures, that the new BIOS works correctly and that all chipset registers, which were saved in the setup, are reinitialized through the BIOS. DMI should only be erased (option /cd) if the BIOS supplier advises to do so.
A complete description of all valid parameters is shown with the parameter “/?”.
In order to make the updating process run automatically, the parameter “/py” must be added. This parameter bypasses all security checks during programming.

CAUTION

Updating the BIOS in an improper way can render the board unusable. Therefore, you should only update the BIOS if you really need the changes/corrections which come with the new BIOS version.

CAUTION

Before you proceed to update the BIOS you need to make absolutely sure that you have the right BIOS file which was issued for the exact board and exact board revision that you wish to update. If you try to update the BIOS using the wrong file the board will not start up again.

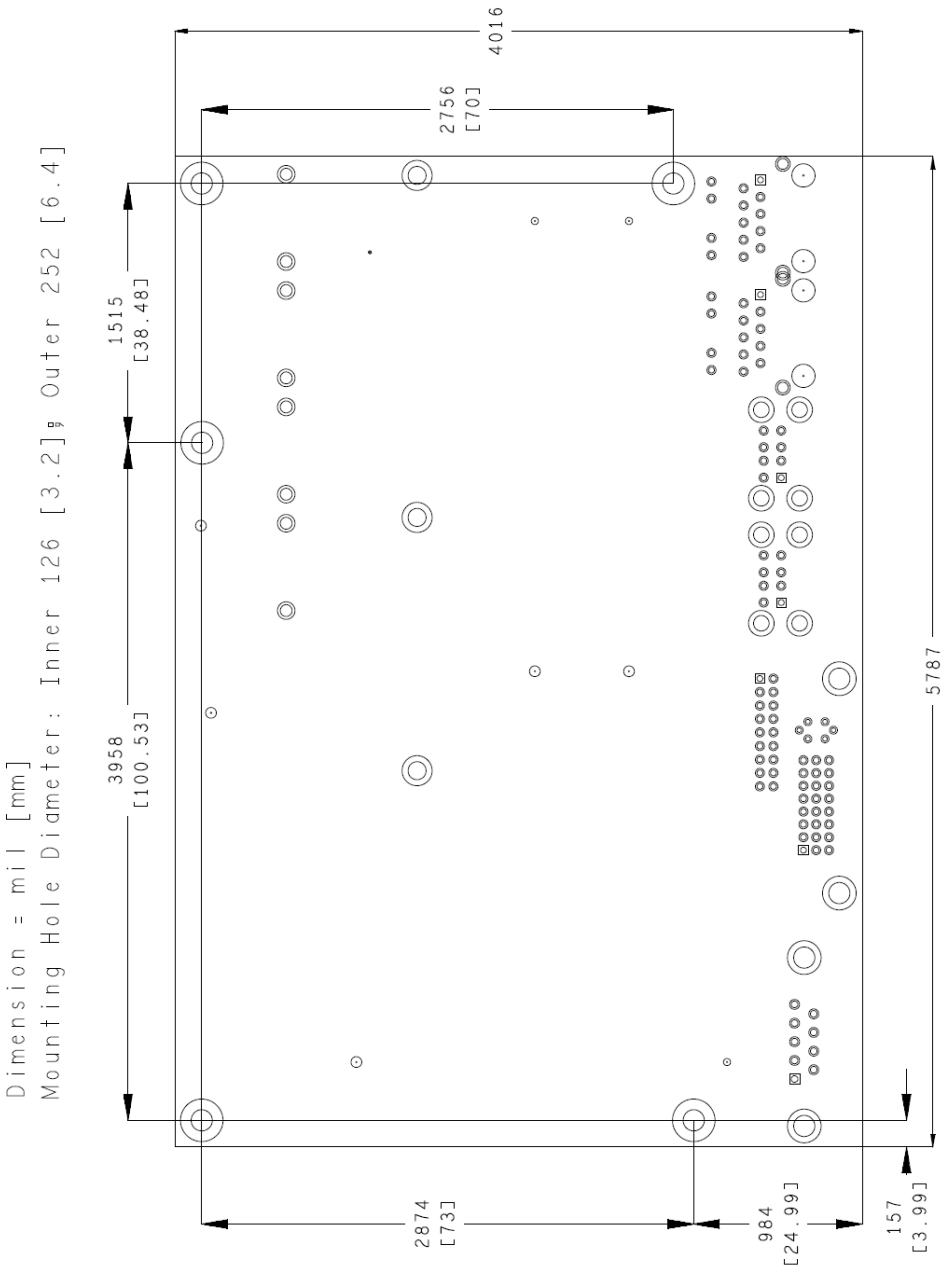
6 Mechanical Drawings

6.1 PCB: Mounting Holes

A true dimensioned drawing can be found in the PC/104 specification.

NOTE

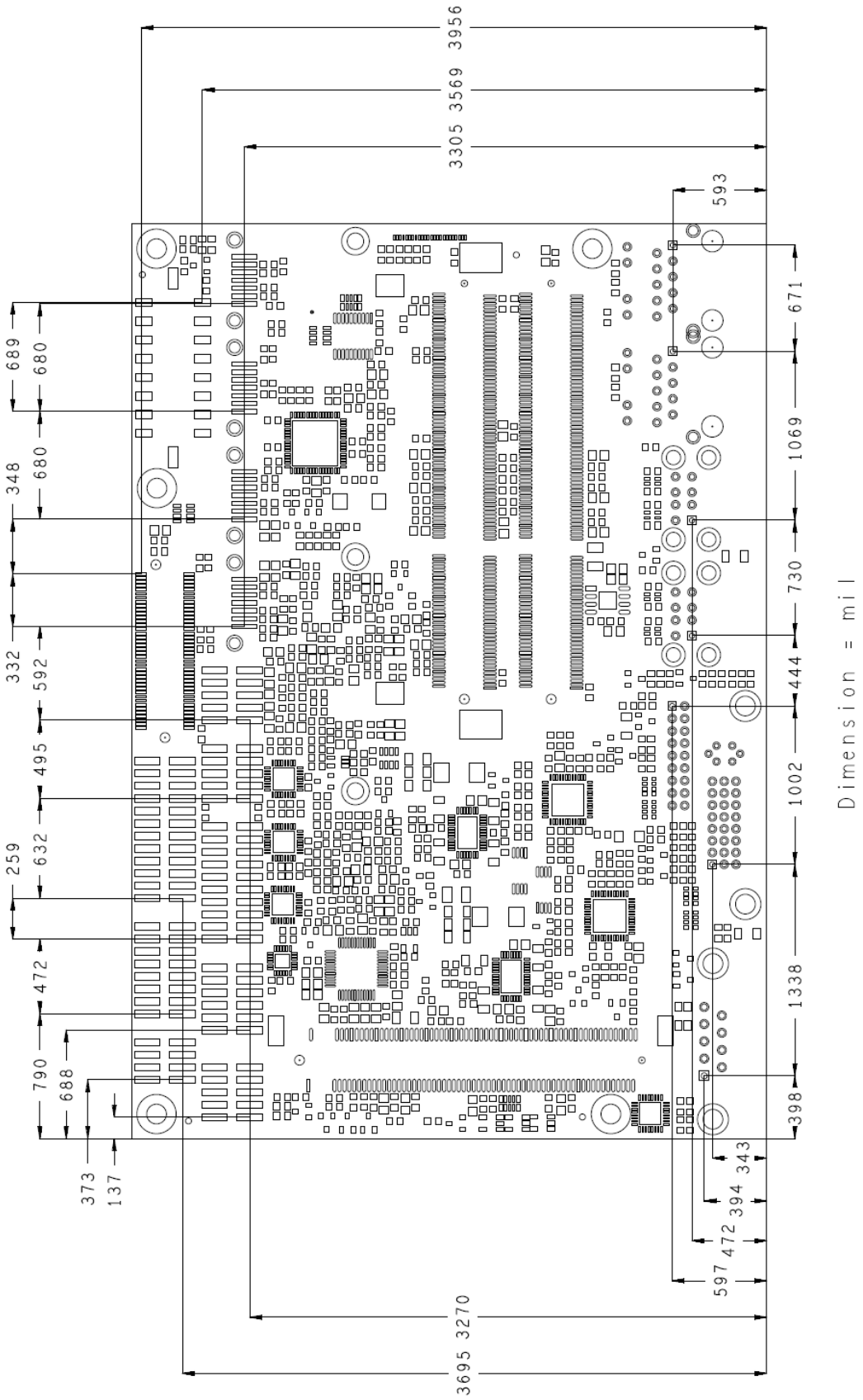
All dimensions are in mil (1 mil = 0,0254 mm)



6.2 PCB: Pin 1 Dimensions

NOTE

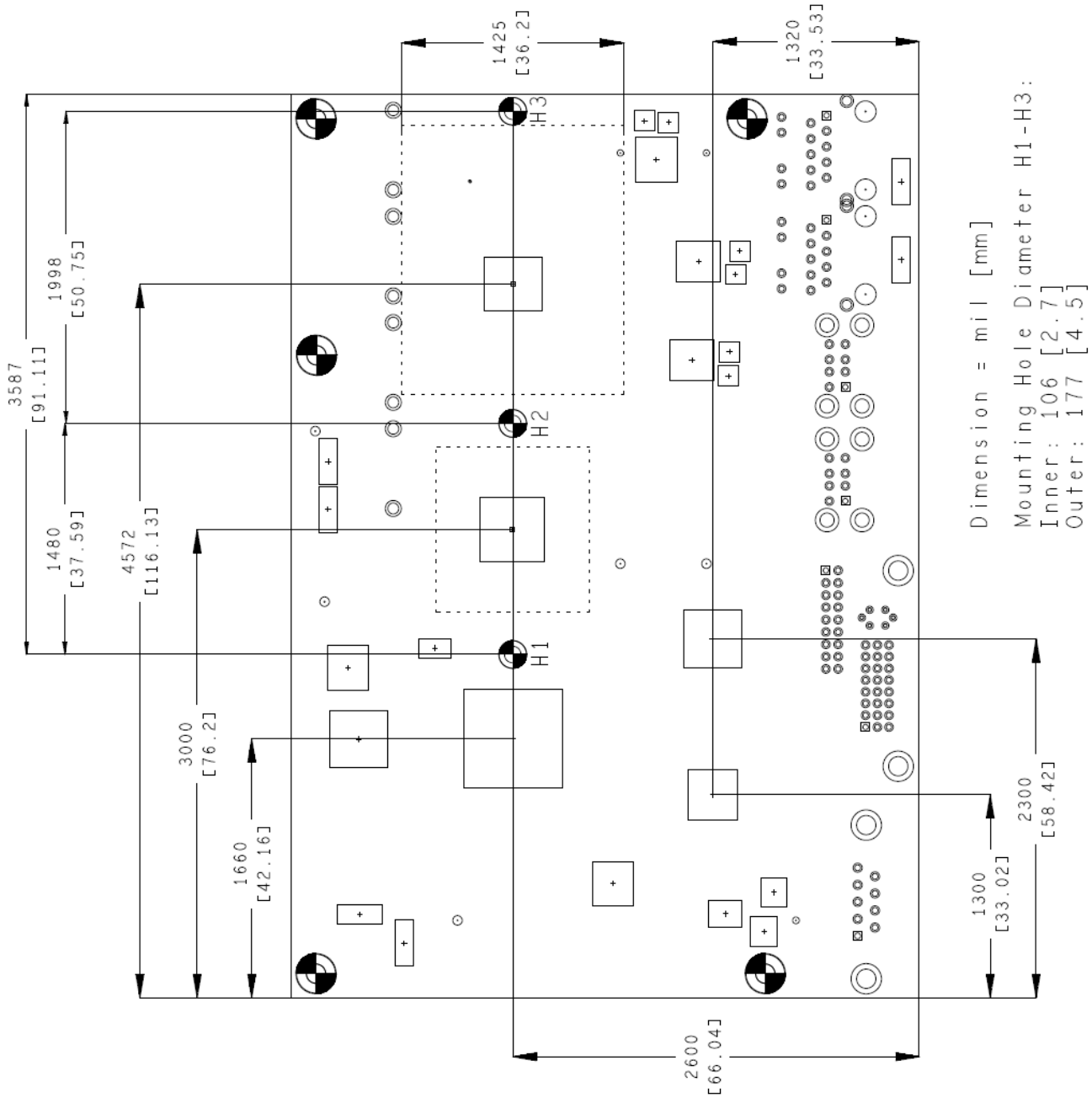
All dimensions are in mil (1 mil = 0,0254 mm)



6.3 PCB: Die Center

NOTE

All dimensions are in mil (1 mil = 0,0254 mm)



7 Technical Data

7.1 Electrical Data

Power Supply:

Board:	5 Volt +/- 5% (5 Volt Suspend / 12 Volt Fan)
RTC:	>= 3 Volt

Electric Power Consumption:

RTC:	<= 10µA

7.2 Environmental Conditions

Temperature Range:

Operating:	0°C to +60°C (extended temperature on request)
Storage:	-25°C up to +85°C
Shipping:	-25°C up to +85°C, for packaged boards

Temperature Changes:

Operating:	0.5°C per minute, 7.5°C per 30 minutes
Storage:	1.0°C per minute
Shipping:	1.0°C per minute, for packaged boards

Relative Humidity:

Operating:	5% up to 85% (non condensing)
Storage:	5% up to 95% (non condensing)
Shipping:	5% up to 100% (non condensing), for packaged boards

Shock:

Operating:	150m/s^2, 6ms
Storage:	400m/s^2, 6ms
Shipping:	400m/s^2, 6ms, for packaged boards

Vibration:

Operating:	10 up to 58Hz, 0.075mm amplitude
	58 up to 500Hz, 10m/s^2
Storage:	5 up to 9Hz, 3.5mm amplitude
	9 up to 500Hz, 10m/s^2
Shipping:	5 up to 9Hz, 3.5mm amplitude
	9 up to 500Hz, 10m/s^2, for packaged boards

CAUTION

Shock and vibration figures pertain to the motherboard alone and do not include additional components such as heat sinks, memory modules, cables etc.

7.3 Thermal Specifications

The board is specified to operate in an environmental temperature range from 0°C to +60°C (extended temperature on request). Maximum die temperature is 105°C. To keep the processor under this threshold an appropriate cooling solution needs to be applied. This solution has to take typical and maximum power consumption into account. The maximum power consumption may be twice as high and should be used as a basis for the cooling concept. Additional controllers may also affect the cooling concept. The power consumption of such components may be comparable to the consumption of the processor.
The board design includes thermal solution mounting points that will provide the best possible thermal interface between die and solution. Since we take thermal solutions seriously we have several advanced, aggressive cooling solutions in our product portfolio. Please contact your sales representative to order or discuss your thermal solution needs.

CAUTION

The end customer has the responsibility to ensure that the die temperature of the processor does not exceed 105°C. Permanent overheating may destroy the board!
In case the temperature exceeds 105°C the environmental temperature must be reduced. Under certain circumstances sufficient air circulation must be provided.

8 Support and Service

Beckhoff and their partners around the world offer comprehensive support and service, making available fast and competent assistance with all questions related to Beckhoff products and system solutions.

8.1 Beckhoff's Branch Offices and Representatives

Please contact your Beckhoff branch office or representative for local support and service on Beckhoff products.
The addresses of Beckhoff's branch offices and representatives around the world can be found on her internet pages: http://www.beckhoff.com
You will also find further documentation for Beckhoff components there.

8.2 Beckhoff Headquarters

Beckhoff Automation GmbH
Eiserstr. 5
33415 Verl
Germany

phone: +49(0)5246/963-0
fax: +49(0)5246/963-198
e-mail: info@beckhoff.com
web: www.beckhoff.com

8.2.1 Beckhoff Support

Support offers you comprehensive technical assistance, helping you not only with the application of individual Beckhoff products, but also with other, wide-ranging services:

- support
- design, programming and commissioning of complex automation systems
- and extensive training programs for Beckhoff system components

hotline: +49(0)5246/963-157
fax: +49(0)5246/963-9157
e-mail: support@beckhoff.com

8.2.2 Beckhoff Service

The Beckhoff Service Center supports you in all matters of after-sales service:

- on-site service
- repair service
- spare parts service
- hotline service

hotline: +49(0)5246/963-460
fax: +49(0)5246/963-479
e-mail: service@beckhoff.com

I Annex: Post-Codes

Code	Description
01h	The Xgroup-program code is written in the random access memory from address 1000:0 onwards.
03h	Initialise Variable/Routine "Superio_Early_Init".
05h	1. Cancel display 2. Cancel CMOS error flag
07h	1. Cancel 8042 (keyboard controller) Interface Register 2. Initialising and self testing of 8042 (keyboard controller)
08h	1. Test of special keyboard controllers (Winbond 977 super I/O Chip-series). 2. Enabling of the keyboard-interface register
0Ah	1. Disabling of the PS/2 mouse interface (optional). 2. Auto-detection of the connectors for Keyboard and mouse, optional: swap of PS/2 mouse ports and PS/2 interfaces.
0Eh	Test of the F000h-memory segment (Read/Write ability). In case of an error a signal will come out of the loud speakers.
10h	Auto-detection of the flash-rom-type and loading of the suitable Read/Write program into the run time memory segment F000 (it is required for ESCD-data & the DMI-pool-support).
12h	Interface-test of the CMOS RAM-logic (walking 1's"-algorithm). Setting of the power status of the real-time-clock (RTC), afterwards test of register overflow.
14h	Initialising of the chip-set with default values. They can be modified through a software (MODBIN) by the OEM-customer.
16h	Initialise Variable/Routine "Early_Init_Onboard_Generator".
18h	CPU auto-detection (manufacturer, SMI type (Cyrix or Intel), CPU-class (586 or 686).
1Bh	Initialising if the interrupt pointer table. If nothing else is pretended, the hardware interrupts will point on "SPURIOUS_INT_HDLR and the software interrupts will point on SPURIOUS_soft_HDLR.
1Dh	Initialise Variable/Routine EARLY_PM_INIT.
1Fh	Load the keyboard table (Notebooks)
21h	Initialising of the hardware power management (HPM) (Notebooks)
23h	1. Test the validity of the RTC-values (Example: "5Ah" is an invalid value for an RTC-minute). 2. Load the CMOS-values into the BIOS Stack. Default-values are loaded if CMOS-checksum errors occur. 3. Preparing of the BIOS 'resource map' for the PCI & plug and play configuration. If ESCD is valid, take into consideration the ESCD's legacy information. 4. Initialise the onboard clock generator. Clock circuit at non-used PCI- and DIMM slots. 5. First initialising of PCI-devices: assign PCI-bus numbers - alot memory- & I/O resources - search for functional VGA-controllers and VGA-BIOS and copy the latter into memory segment C000:0 (Video ROM Shadow).
27h	Initialise cache memory for INT 09
29h	1. Program the CPU (internal MTRR at P6 and PII) for the first memory address range (0-640K). 2. Initialising of the APIC at CPUs of the Pentium-class. 3. Program the chip-set according to the settings of the CMOS-set-up (Example: Onboard IDE-controller). 4. Measuring of the CPU clock speed. 5. Initialise the video BIOS.
2Dh	1. Initialise the "Multi-Language"-function of the BIOS 2. Soft copy, e.g. Award-Logo, CPU-type and CPU clock speed…
33h	Keyboard-reset (except super I/O chips of the Winbond 977 series)
3Ch	Test the 8254 (timer device)
3Eh	Test the interrupt Mask bits of IRQ-channel 1 of the interrupt controller 8259.
40h	Test the interrupt Mask bits of IRQ-channel 2 of the interrupt controller 8259
43h	Testing the function of the interrupt controller (8259).
47h	Initialise EISA slot (if existent).

Code	Description
49h	1. Determination of the entire memory size by revising the last 32-Bit double word of each 64k memory segment. 2. Program “write allocation” at AMD K5-CPUs.
4Eh	1. Program MTRR at M1 CPUs 2. Initialise level 2-cache at CPUs of the class P6 and set the “cacheable range” of the random access memory. 3. Initialise APIC at CPUs of the class P6. 4. Only for multiprocessor systems (MP platform): Setting of the “cacheable range” on the respective smallest value (for the case of non-identical values).
50h	Initialise USB interface
52h	Testing of the entire random access memory and deleting of the extended memory (put on “0”)
55h	Only for multi processor systems (MP platform): Indicate the number of CPUs.
57h	1. Indicate the plug and play logo 2. First ISA plug and play initialising – CSN-assignment for each identified ISA plug and play device.
59h	Initialise TrendMicro anti virus program code.
5Bh	(Optional:) Indication of the possibility to start AWDFLASH.EXE (Flash ROM programming) from the hard disk.
5Dh	1. Initialise Variable/Routine Init_Onboard_Super_IO. 2. Initialise Variable/Routine Init_Onbaord_AUDIO.
60h	Release for starting the CMOS set-up (this means that before this step of POST, users are not able to access the BIOS set-up).
65h	Initialising of the PS/2 mouse.
67h	Information concerning the size of random access memory for function call (INT 15h with AX-Reg. = E820h).
69h	Enable level 2 cache
6Bh	Programming of the chip set register according to the BIOS set-up and auto-detection table.
6Dh	1. Assignment of resources for all ISA plug and play devices. 2. Assignment of the port address for onboard COM-ports (only if an automatic junction has been defined in the setup).
6Fh	1. Initialising of the floppy controller 2. Programming of all relevant registers and variables (floppy and floppy controller).
73h	Optional feature: Call of AWDFLASH.EXE if: - the AWDFLASH program was found on a disk in the floppy drive. - the shortcut ALT+F2 was pressed.
75h	Detection and installation of the IDE drives: HDD, LS120, ZIP, CDROM…
77h	Detection of parallel and serial ports.
7Ah	Co-processor is detected and enabled.
7Fh	1. Switch over to the text mode, the logo output is supported. - Indication of possibly emerged errors. Waiting for keyboard entry. - No errors emerged, respective F1 key was pressed (continue): Deleting of the EPA- or own logo.
82h	1. Call the pointer to the “chip set power management”. 2. Load the text font of the EPA-logo (not if a complete picture is displayed) 3. If a password is set, it is asked here.
83h	Saving of the data in the stack, back to CMOS.
84h	Initialising of ISA plug and play boot drives (also Boot-ROMs)
85h	1. Final initialising of the USB-host. 2. At network PCs (Boot-ROM): Construction of a SYSID structure table 3. Backspace the scope presentation into the text mode 4. Initialise the ACPI table (top of memory). 5. Initialise and link ROMs on ISA cards 6. Assignment of PCI-IRQs 7. Initialising of the advanced power management (APM) 8. Set back the IRQ-register.

Code	Description
93h	Reading in of the hard disk boot sector for the inspection through the internal anti virus program (trend anti virus code)
94h	1. Enabling of level 2 cache 2. Setting of the clock speed during the boot process 3. Final initialising of the chip set. 4. Final initialising of the power management. 5. Erase the onscreen and display the overview table (rectangular box). 6. Program “write allocation” at K6 CPUs (AMD) 7. Program “write combining” at P6 CPUs (INTEL)
95h	1. Program the changeover of summer-and winter-time 2. Update settings of keyboard-LED and keyboard repeat rates
96h	1. Multi processor system: generate MP-table 2. Generate and update ESCD-table 3. Correct century settings in the CMOS (20xx or 19xx) 4. Synchronise the DOS-system timer with CMOS-time 5. Generate an MSIRQ-Routing table..
C0h	Chip set initialising: - Cut off shadow RAM - Cut off L2 cache (apron 7 or older) - Initialise chip set register
C1h	Memory detection: Auto detection of DRAM size, type and error correction (ECC or none) Auto detection of L2 cache size (apron 7 or older)
C3h	Unpacking of the packed BIOS program codes into the random access memory.
C5h	Copying of the BIOS program code into the shadow RAM (segments E000 & F000) via chipset hook.
CFh	Testing of the CMOS read/write functionality
FFh	Boot trial over boot-loader-routine (software-interrupt INT 19h)

II Annex: Resources

IO Range

The used resources depend on setup settings.
The given values are ranges, which are fixed by AT compatibility. Other IO ranges are used, which are dynamically adjusted by Plug & Play BIOS while booting.

Address	Function
0-FF	Reserved IO area of the board
170-17F	
1F0-1F7	
278-27F	
2E8-2EF	COM4
2F8-2FF	COM2
370-377	
378-37F	
3BC-3BF	
3E8-3EF	COM3
3F0-3F7	
3F8-3FF	COM1

Memory Range

The used resources depend on setup settings.
If the entire range is clogged through option ROMs, these functions do not work anymore.

Address	Function
A0000-BFFFF	VGA RAM
C0000-CFFFF	VGA BIOS
D0000-DFFFF	AHCI BIOS / RAID / PXE (if available)
E0000-EFFFF	System BIOS while booting
F0000-FFFFF	System BIOS

Interrupt

The used resources depend on setup settings.
The listed interrupts and their use are given through AT compatibility.
If interrupts must exclusively be available on the ISA side, they have to be reserved through the BIOS setup.
The exclusivity is not given and not possible on the PCI side.

Address	Function
IRQ0	Timer
IRQ1	PS/2 Keyboard
IRQ2 (9)	COM3
IRQ3	COM1
IRQ4	COM2
IRQ5	COM4
IRQ6	
IRQ7	
IRQ8	RTC
IRQ9	
IRQ10	
IRQ11	
IRQ12	PS/2 Mouse

Address	Function
IRQ13	FPU
IRQ14	
IRQ15	

PCI Devices

All listed PCI devices exist on the board. Some PCI devices or functions of devices may be disabled in the BIOS setup. Once a device is disabled other devices may get PCI bus numbers different from the ones listed in the table.

AD	INTA	REQ	Bus	Dev.	Fct.	Controller / Slot
	-	-	0	0	0	Host Bridge ID2A40h
	A	-	0	2	0	VGA Graphics ID2A42h
	A	-	0	25	0	LAN ICH9 ID10F5h
	A	-	0	26	0	USB UHCI Controller #4 ID2937h
	B	-	0	26	1	USB UHCI Controller #5 ID2938h
	D	-	0	26	2	USB UHCI Controller #6 ID2939h
	C	-	0	26	7	USB 2.0 EHCI Controller #2 ID293Ch
	A	-	0	27	0	HDA Controller ID293Eh
	A	-	0	28	0	PCI Express Port 1 ICH9 ID2940h
	B	-	0	28	1	[PCI Express Port 2 ICH9 ID2942h]
	C	-	0	28	2	[PCI Express Port 3 ICH9 ID2944h]
	D	-	0	28	3	[PCI Express Port 4 ICH9 ID2946h]
	A	-	0	28	4	PCI Express Port 5 ICH9 ID2948h
	A	-	0	29	0	USB UHCI Controller #1 ID2934h
	B	-	0	29	1	USB UHCI Controller #2 ID2935h
	C	-	0	29	2	USB UHCI Controller #3 ID2936h
	A	-	0	29	7	USB 2.0 EHCI Controller #1 ID293Ah
	-	-	0	30	0	DMI-to-PCI Bridge ID2448h
	-	-	0	31	0	LPC Interface ID2917h
	B	-	0	31	2	SATA Interface #1 ID2928h
	B	-	0	31	3	SMBus Interface ID2930h
	B	-	0	31	5	SATA Interface #2 ID292Dh
	A	-	m	0	0	LAN 82547L ID10D3h
21	A	0	n	5	0	mPCI Slot 1

SMB Devices

The following table contains all reserved SM-Bus device addresses in 8-bit notation. Note that external devices must not use any of these addresses even if the component mentioned in the table is not present on the motherboard.

Address	Function
10-11	Standard slave address
40-41	GPIO
60-61	BIOS internal
70-73	POST code output
88-89	BIOS-defined slave address
A0-A1	DIMM 1
A2-A3	DIMM 2
A4-AF	BIOS internal

Address	Function
B0-BF	BIOS internal
D2-D3	Clock